Code: AE-27 **Subject: DIGITAL HARDWARE DESIGN**

JUNE 2007

Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. VHDL, stands for

(A) Verilog Hardware Description Langauge
(B) Very High Speed Device Language
(C) Versatile Hardware Description Language
(D) Very High Speed Integrated Circuit Hardware Description Language

b. "The main module is described as the interconnection of simpler modules (hierarchical description)". This statement discuss

(A) Behavioural Architecture **(B)** Data flow Architecture
(C) Structural Architecture **(D)** None of the above

c. Two numbers with digits X and Y and radix 5 and 4 have following relationship: $(XY)_5 = (YX)_4$ then

(A) X=4, Y=3 **(B)** X=4, Y=3
(C) X=6, Y=3 **(D)** X=3, Y=4

d. Arrange the microinstruction execution cycle
1. Fetch 2. Execute 3. Decode 4. calculate the address of next

(A) 1-2-3-4 **(B)** 1-3-2-4
(C) 2-1-3-4 **(D)** 2-3-1-4

e. Typical elements of a SRAM-controlled FPGA are:

(A) Programmable switches and multiplexers
(B) Look-up tables
(C) Flip-Flops
(D) All of the above

f. Hamming code for the decimal digit 4 coded in BCD is

(A) 1001100 **(B)** 1000100
(C) 0010100 **(D)** 1101100

g. The circuit shown in Fig.1 detects the following sequence

(A) 0111 **(B)** 0000
(C) 0101 **(D)** 1111

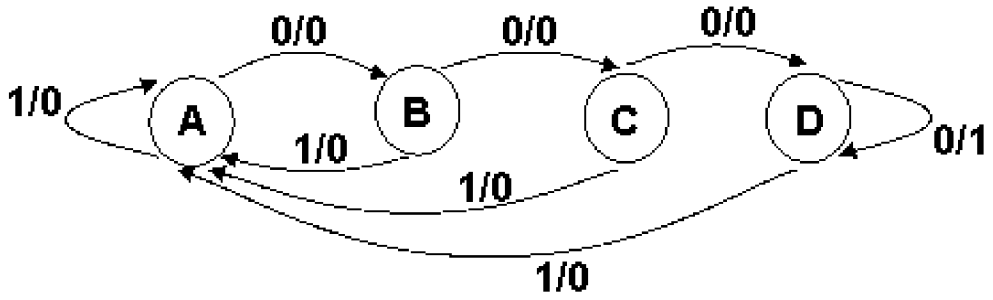

Fig. 1

h. The correct answer of the simplified form of the Boolean equation
T(x,y,z) = (x+y) [x'(y'+z')] + x'y' + x'z' is

(A) 0 **(B)** 1
(C) x+y' **(D)** y'+z'

i. Compare to Vertical control field format, Horizontal control field format:

(A) is faster in generation of the control signal
(B) is inefficient in memory space usage
(C) requires no decoding
(D) All of the above

j. A multiplier multiplies N bit binary number by M bit binary number, the bit size of the result is

(A) N x M **(B)** N^2
(C) M^2 **(D)** N+M

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Briefly explain the following:

(i) Races

(ii) Package declaration in VHDL

(iii) Unate function

(iv) Explicit sequencing **(2+2+2+2=8)**

b. Find the prime implicates of the function

$f(x_3, x_2, x_1, x_0) = zero\text{-}set\ (7,13,15)$. **(4)**

c. Design a minimal gate network for a combinational system specified as follows:

Input: $x \in \{0, 1, 2, ..., 9\}$ coded in BCD as

$\underline{x} = (x_3, x_2, x_1, x_0), x_i \in \{0, 1\}$

Output: $z \in \{0, 1\}$

Function: $$z = \begin{cases} 1 & \textbf{if} \quad x \in \{0, 2, 3, 5, 8\} \\ 0 & \textbf{otherwise} \end{cases}$$

(4)

Q.3 a. What do you mean by functional decomposition? Explain serial and parallel decomposition. **(8)**

b. Define symmetric function and find whether the function

F (w,x,y,z) = $\sum$ (0,1,3,5,8,10,11,12,13,15) is symmetric. If it is so express the function in symmetric notation.

(8)

Q.4 a. Discuss relationship between system specification and implementation of digital system. **(3)**

b. Briefly explain the following:

(i) FPGA

(ii) Modulo K counter **(6)**

c. Determine whether the function

f(x1,x2,x3,x4) = $\sum$ (0,1,3,4,5,6,7,12,13,) is a threshold function, and if it is, find a weight-threshold vector. **(7)**

Q.5 a. Discuss importance and classification of data paths. **(6)**

b. Design a synchronous sequential circuit, which is required to produce an output pulse z=1,

whenever the sequence 1111 occurs. Overlapping sequences are accepted. For example, if the input is 01011111……, the required output is 00000011.

(i) Draw a state diagram.

(ii) Select an assignment and show the excitation and output tables

(iii) Write down the excitation functions for SR flip-flops, and draw the corresponding logic diagram. **(10)**

Q.6 a. Implement a four bit adder using a 512 X 5 ROM module. **(4)**

b. Draw an ASM chart to detect the sequence 0101. **(6)**

c. Implement six input decoder using co-incident and tree decoder networks. **(6)**

Q.7 Write the VHDL code for the following:

(i) Write a VHDL code for D flip-flop with asynchronous clear and preset using behavioural approach.

(ii) Write a VHDL code for one bit full adder using data flow architecture. Extend it to 4 bit adder using structural approach.

(iii) Write a VHDL code for 4-bit shifter with following features:
(a) parallel Load (b) left right shift control **(4+6+6)**

Q.8 a. Discuss Ring counter in detail. Modify Rig counter to make it Twisted-tail ring counter. **(6)**

b. For the following machine shown in Table 1, find the equivalence partition and a corresponding reduce machine in standard form. Also solve same problem with merger graph method. **(10)**

PS	NS, Z	
	X=0	X=1
A	F, 0	B, 0
B	F, 0	A, 0
C	E, 0	B, 1
D	E, 0	A, 1
E	C, 0	F, 1
F	B, 0	C, 0

Table 1

Q.9 Write explanatory notes on (Any **FOUR)**

(i) Hazard free asynchronous circuits

(ii) Structural style of Modeling in VHDL

(iii) Incompletely specified machine

(iv) Compare Moore Model and Melay model with example

(v) Merits and Demerits of Programmable modules. **(4 × 4)**