SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act,1956)

Course & Branch :B.E - EEE/P-ECE/P-EEE
Title of the Paper :Analog Integrated Circuits — Max. Marks :80
Sub. Code :6C0080/6CPT0027 — Time : 3 Hours
Date :06/05/2010 — Session :FN

PART - A (10 x 2 = 20)

Answer ALL the Questions

1. Define CMRR?

2. What is the need for frequency compensation?

3. Draw a circuit to find $V_0 = (V_1 + V_2) – (V_3 + V_4)$

4. What is meant by hysterisis in a Schmitt trigger circuit?

5. Define lock range and capture range in PLL.

6. What is the principle of VCO?

7. Why is an inverted R-2R ladder network DAC better than R-2R ladder DAC?

8. What are analog switches?

9. What is opto coupler?

10. What is the output voltage of each of the following IC regulators?
    (a) 7806 (b) 7905 (c) 7818 (d) 7921

PART – B (5 x 12 = 60)

Answer All the Questions

11. (a) Explain in detail about the current mirror circuit.
    (b) Analyse the differential amplifier with active load.

(or)

12. (a) Define Slew rate and explain in detail the methods of improving slew rate.
    (b) Explain the frequency compensation techniques in detail.

13. With neat sketches of circuit diagram, write short notes on
    (a) Integrator (b) Differentiator (c) Log amplifiers.

(or)

14. Explain the following circuits with neat diagrams.
    (a) Instrumentation amplifier (8)
    (b) Triangular wave generator (4)

15. Explain four quadrant variable transconductance multiplier.

(or)

16. Explain the operation of PLL with its block diagram and explain its applications.

17. With a neat sketch explain successive approximation ADC.

(or)

18. Explain the following
    (a) Voltage to time converter (b) Voltage to frequency converter

19. Draw and explain the functional diagram of 555 timer and give its applications.

(or)

20. With neat sketch, explain
    (a) Switched capacitor filter
    (b) Tuned amplifiers.