SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E – EEE
Title of the paper: Digital Systems
Semester: IV — Max. Marks: 80
Sub.Code: 6C0038 — Time: 3 Hours
Date: 02-05-2008 — Session: FN

PART – A (10 x 2 = 20)

Answer All the Questions

1. What is an alphanumeric code?
2. Multiply 1011_2 by 101_2
3. What do you mean by parity check?
4. Give applications of PLA.
5. What will be the maximum number of outputs for a decoder with a 6 bit data word?
6. What do you understand by Demultiplexer?
7. What is a FF? What are the characteristics of FFs?
8. How are shift registers useful?
9. What is open collector output TTL? Where is it used?
10. What are the different logic families that exhibit low power dissipation?

PART – B (5 x 12 = 60)

Answer All the Questions

11. (a) Prove that:
    (i) $X + YZ = (X+Y)(X+Z)$ (2)
    (ii) $X.\overline{Y} + Y = X + Y$ (2)

(b) Conver 427_8 to decimal, binary and hexa (4)

(c) Convert $1A53_{16}$ to other systems (4)

(or)

12. (a) Convert $110A.AB_H$ tpo decimal, binary and octal.
(b) Explain the process of Multiple output minimization.
(c) Solve using 3 variable mapping
$F = m3 + Dm2 + m6 + m4 + d(m0 + \overline{D}m7)$ (d – don't care)

13. Obtain the minimum SOP and verify using K map.

(or)

14. (a) Determine to prime implications of
$F(A,B,C,D) = \Sigma(3,4,5,7,9,13,14,15)$ (9)
(b) What do you understand by variable mapping? (3)

15. Design a synchronous counter using JK FF to count to following sequence. 7,4,3,1,5,0,7…….

(or)

16. Design a decimal to BCD priority encoder.

17. Design a mod-6 counter using FFS. Draw the state transition diagram of the same.

(or)

18. Design a mod-6 counter using FFs. Draw the state transition diagram of the same.

19. Explain the following logics in detail.
(a) HTL
(b) CMOS

(or)

20. Write notes on the following:
(a) SRAM
(b) CCD
(C) PAL