Code: A-09/C-03/T-03
Subject: ANALOG & DIGITAL ELECTRONICS
Time: 3 Hours
Max. Marks: 100

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x8)

a. For the circuit shown in Fig.1, the input resistance R_{id} will be

(A) $2R_1$. **(B)** $2R_1 + R_2$.

(C) $2(R_1 + R_2)$. **(D)** Infinity.

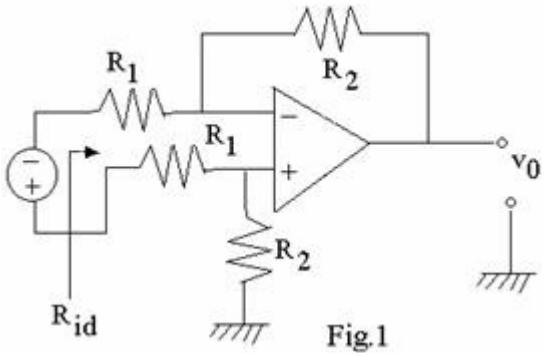

Fig.1

b. A second order filter has its poles at $s = -\frac{1}{2} \pm j\frac{\sqrt{3}}{2}$. The transmission is zero at $\omega = 2\ \text{rad/s}$ and is unity at $\omega = 0$. The transfer function of the filter is

(A) $\frac{1}{4}\frac{(s^2 + s)}{(s^2 - s + 1)}$. **(B)** $\frac{1}{4}\frac{(s^2 + s)}{(s^2 + s + 1)}$.

(C) $\frac{1}{4}\frac{(s^2)}{(s^2 + s + 0.25)}$. **(D)** $\frac{1}{4}\frac{(s^2 - s)}{(s^2 - s - 1)}$.

c. Transfer function of a filter is given by $T(s) = \frac{a_1 s}{s^2 + \frac{\omega_0}{Q} s + \omega_o^2}$. It represents a _____filter.

(A) Low pass. **(B)** High pass.
(C) Band pass. **(D)** Band stop.

d. The circuit shown below in Fig.2

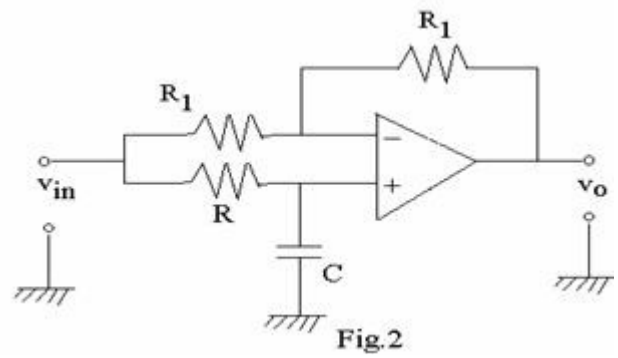

Fig.2

represents _____ filter.

(A) Low pass. **(B)** High pass.
(C) Band pass. **(D)** All pass.

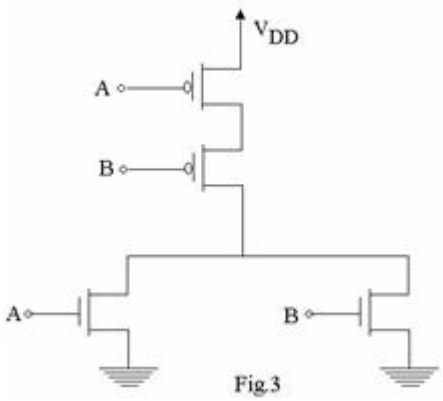

Fig.3

e. The circuit shown in Fig.3 below represents _____ gate

(A) AND.
(B) NAND.
(C) OR.
(D) NOR.

f. Active loaded MOS differential circuit has a

(A) high CMRR. **(B)** low CMRR.
(C) high delay. **(D)** high differential gain.

g. NPN transistor is not suitable for good analog switch because

(A) $I_C - V_{CE}$ characteristic curve pass directly through origin.
(B) the device has very high input impedance.
(C) the device is asymmetrical with an offset voltage V_{CE} off.
(D) it has well defined transition frequency f_T.

h. CMOS logic has the property of

(A) increased capacitance and delay. **(B)** decreased area.
(C) high noise margin. **(D)** low static power dissipation.

PART I

Answer any THREE Questions. Each question carries 14 marks.

Q.2 a. Explain Miller Integrator. What are the effects of the OP-AMP input offset voltage, input bias and offset currents on the performance of Miller Integrator. **(7)**

b. Consider a symmetrical square wave of 20V peak to peak, zero average and 2ms period applied to a Miller integrator. Find the value of the time constant (CR) such that the triangular waveforms at the output has 20V peak to peak amplitude. **(7)**

Q.3 a. Draw the circuit diagram of two stage CMOS op-amp configuration. What do you understand by systematic output dc offset voltage? How can it be eliminated? **(8)**

b. Draw the circuit diagram of a CMOS inverter and explain its operation. **(6)**

Q.4 The transfer function of a two port network is given by $T(s) = \frac{z_2}{z_1 + z_2}$ where z_1 and z_2 represent any impedances. Explain how the following passive filters can be realized from this network.

(i) Bandpass filter. **(4)**
(ii) Notch filter. **(5)**
(iii) All pass filter. **(5)**

Q.5 a. With proper diagram explain the operation of dual slope A/D converter and charge redistribution A/D converter. Compare their advantages and disadvantages. **(10)**

b. Explain the operation of sample & hold circuit. Discuss its applications. **(4)**

Q.6 a. What types of doping should be used in a switching diode. What is reverse recovery time? **(4)**

b. Explain the operation of a MOSFET analog switch with suitable circuit diagram. **(6)**

c. What property of Schottky diode make it suitable for fast switching? Explain . **(4)**

PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 Implement the following Boolean expressions by synthesizing Pull up and Pull down networks:

(i) $Y = \overline{AB}$. **(4)**

(ii) $Y = \overline{A(B + CD)}$. **(5)**

(iii) $Y = A\overline{B} + \overline{A}B$. **(5)**

Q.8 a. Explain the following logic families and compare their performances. **(9)**

(i) ECL. (ii) TTL

b. How ECL and TTL logic families are interfaced with each other. **(5)**

Q.9 a. With a suitable circuit diagram explain how a four bit binary full adder works. How this 4-bit adder can be used as substracter. **(8)**

b. Explain the operation of a BCD to decimal decoder. **(6)**

Q.10 Explain the following with timing diagram.

(i) JK flip-flop. **(7)**

(ii) Clocked SR flip-flop. **(7)**

Q.11 Write short notes on any **TWO** of the following:

(i) Programmable logic Array.

(ii) RAM & PROM.

(iii) Seven segment display system.

(iv) Shift register. **(7+7)**