Code: A-09/C-03/T-03 **Subject: ANALOG & DIGITAL ELECTRONICS**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: **(2x8)**

a. a. The magnitude response $|H(j\omega)|$ of a Butterworth filter of order N has maximally flat characteristics because

(A) first N derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = 0$.

(B) first N-1derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = 0$.

(C) (C) first N-1 derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = \infty$.

(D) (D) first N derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = \infty$.

b. b.

Input impedance of the OpAmp circuit shown in the fig

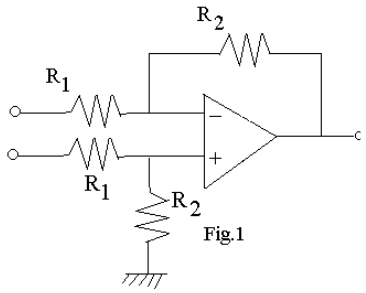


Fig.1

(A) (A) $R_2 + 2R_1$

(B) (B) $R_2 + \frac{R_1}{2}$.

(C) (C) $2R_1$.

(D) (D) $\frac{R_1}{2}$.

c. Output V_0 for $V_i = 1V$ dc for the circuit shown in the fig.2 will be

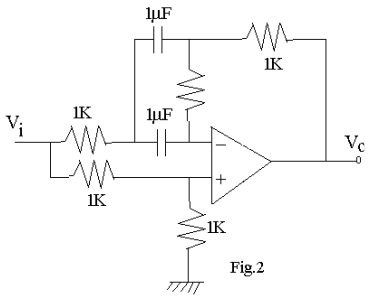


Fig.2

(A) (A) 1.0 V.
(B) (B) -0.5 V.
(C) 0.5 V.
(D) 0.0 V.

d. The Boolean expression $f(A,B,C,D) = \overline{A}C\overline{B} + BC\overline{D} + A\overline{C}D$ can equivalently be written, in terms of its minterms, as

(A) $\sum m(2,3,6,14,9,13)$. **(B)** $\sum m(3,4,6,14,9,13)$.

(C) (C) $\sum m(2,3,6,14,8,12)$. **(D)** $\sum m(2,3,5,15,9,13)$.

e. The T-input of a negative edge triggered has been tied to logic 1. If its clock input is as shown in the fig.3, then ON tively

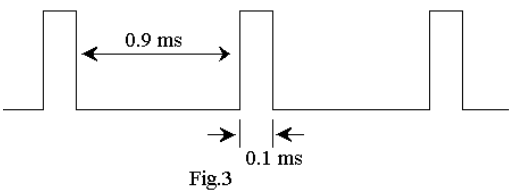
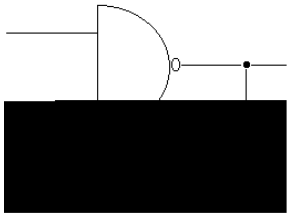


Fig.3

(A) **(A)** 0.2 ms and 1.8 ms.
(B) **(B)** 1.8 ms and 0.2 ms.
(C) 0.5 ms and 0.5 ms.
(D) 1.0 ms and 1.0 ms.

f. Immediately after the inputs to a NAND RS flipflop are simultaneously switched from 00 to 11, the output Q of the flipflop will
(A) **(A)** be equal to 0. **(B)** be equal to 1.
(C) race around. **(D)** be unpredictable.

g. The circuit shown in the fig.4 is a



(A) flipflop.
(B) sequential circuit.
(C) combinational circuit.
(D) parity checker.

h. A MOS differential amplifier has a large gain because
(A) the current through each driver transistor is a constant.
(B) sum of currents through both driver transistors is a constant.
(C) the load is a current source and offers a large resistance.
(D) there is a no feedback in the circuit.

PART I
Answer any THREE Questions. Each question carries 14 marks.

Q.2 The OpAmp shown in the circuit of fig.5 has an open loop gain of 10000, input impedance of 1MΩ and an output impedance of 1KΩ.

(i) Determine $V = V_+ - V_-$ if 2.1V is applied between terminals A and B. **(5)**

(ii) Find the gain $\frac{V_o}{V_i}$ of this amplifier. **(5)**

(iii) Find ce resistance of 1KΩ.

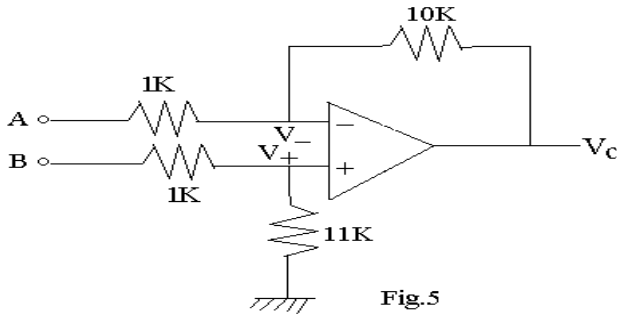


Fig.5

Q.3 Consider the function $H(s) = K\dfrac{s^2 - as + b}{s^2 + as + b}$.

(i) Draw its pole-zero diagram.

(2)

(ii) Sketch magnitude and phase responses of this function.

(4)

(iii) For K=1, draw a passive circuit to realize H(s).

(5)

(iv) Draw a block diagram circuit to realize this function using integrators, summers and multipliers. **(3)**

Q.4 Explain the working of a 12-bit dual-slope analog to digital converter using appropriate diagrams and derive the relevant expression for the digital output. If the input voltage is in range (0V, 10V) and the counter in the converter is given a clock of 1 MHz, determine

(i) (i) the time taken for output of the integrator to reach its maximum value.

(8)

(ii) (ii) conversion time for input voltage = 5V, assuming reference voltage of 10V.

(6)

Q.5 a. Through proper sketches explain the electron density distribution in the base of a n-p-n Bipolar Junction Transistor when

(i) (i) in Active region

(ii) (ii) in Saturation.

How will the explanation be different for a p-n-p transistor?

(6)

b. The input voltage V switches from +5V to 10V in diode circuit shown in the fig.6. Sketch the current through the diode and explain various regions of this waveform. **(8)**

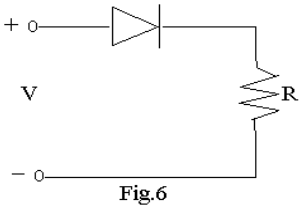


Fig.6

Q.6 With short notes on any **TWO** of the following:

(i) (i) DC level shifting in OpAmps.

(ii) (ii) Sample-and-Hold circuits and their applications.

(iii) (iii) Sensitivity of a single OpAmp Biquad.

(iv) (iv) MOS operational amplifiers.

(14)

PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. A portion of TTL gate circuit is shown in the Fig.7(a), where the transistor Q has $\beta = 100.$ Base-to-emitter voltage of the transistor is equal to 0.7V when it is in active region and 0.75V when Q is in saturation. Determine the output voltage V if the current I=2.5mA.

(6)

b. Both NMOS and PMOS transistors in the circuit of Fig.7(b) have a threshold voltage of 2V and equal characteristic constants. Determine the value of input voltage V_i and the range of output voltage for which both transistors will be in saturation.

(8)

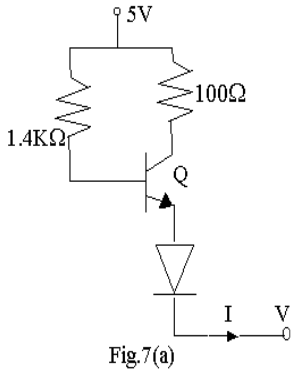


Fig.7(a)

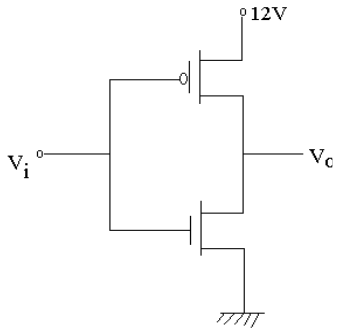


Fig.7(b)

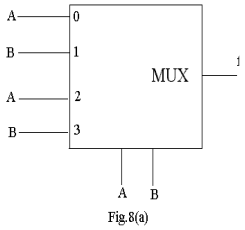


Fig.8(a)

Q.8 a. Determine the Boolean function implemented by the multiplexer circuit shown in the fig.8 (a). **(4)**

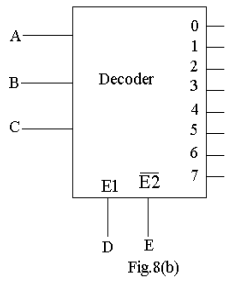
b. A 3-to-8 decoder has two enable inputs E1 and $\overline{E2}$ as shown in fig.8 (b). Write a truth table showing the c 

Fig.8(b)
erms of inputs $A_0 - A_7$.

c. With the help of a diagram using Full-adders, explain the working of a 4-bit parallel addition/subtraction of 2s complement numbers.

(5)

Q.9 a. Explain the working of a positive-edge-triggered Master-Slave JK flipflop. What are its advantages over a normal JK flipflop? If all NAND gates used in the flipflop have a propagation delay of 5 ns, compute the delay of the Master-Slave.

(6)

b. Design a circuit to generate the sequence 100010 using JK flipflops and logic gates as required. **(8)**

Q.10a.What is the fun[illegible]vorking.

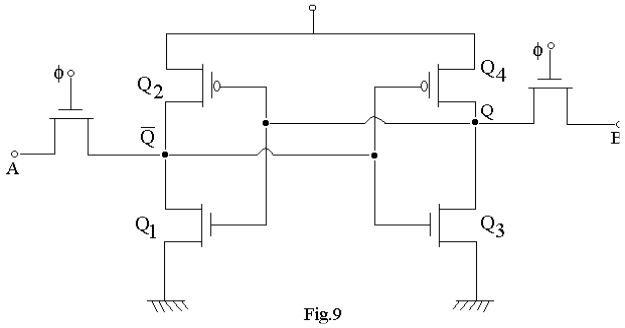


Fig.9

b. Draw the circuit of a CMOS static RAM cell and explain its operation.

(4)

c. Three negative edge triggered flipflops having inputs $J_0\,K_0$, $J_1\,K_1$ and $J_2\,K_2$ respectively, are connected to make a counter such that $J_0 = \overline{Q_2}, K_0 = 1, J_1 = K_1 = 1, J_2 = Q_1Q_0$

Starting with $Q_2Q_1Q_0 = 000$, what sequence(s) of states will the counter go through?

(6)

Q.11 Write short notes on any **THREE** of the following:

(i) (i) Emitter-Coupled OR gate.
(ii) (ii) CMOS logic gates.
(iii) (iii) BJT inverter.
(iv) (iv) Schottky diodes and its applications in digital circuits.

(14)

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