December 2005

Code: A-09

Subject: ANALOG & DIGITAL ELECTRONICS
Time: 3 Hours
Max. Marks: 100

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. The order of input resistance in 741 OPAMP is

(A) 1 to $10^4\Omega$. **(B)** $10^3\Omega$.
(C) $10^5\Omega$. **(D)** $10^6\Omega$.

b. The ratio of change in input offset voltage when variation in supply voltage is made is called

(A) PSRR. **(B)** CMRR .
(C) transient response. **(D)** input offset voltage stability.

c. The equiripple response filter is called _____, while maximally flat time delay response is given by _____ filter.

(A) Chebyshev, Bessel. **(B)** Butter worth, Bessel.
(C) Bessel, Chebyshev. **(D)** Chebyshev, Butter Worth.

d. A notch filter is a

(A) Wide band pass filter. **(B)** Narrow band pass filter.
(C) Wide band reject filter. **(D)** Narrow band reject filter.

e. The problem faced by switched capacitor filters is

(A) aliasing **(B)** amplitude distortion

(C) slower roll off rate **(D)** longer time and phase delay

f. For a 3-bit flash ADC, the number of comparators required are

(A) 5 **(B)** 9
(C) 7 **(D)** 3

g. The typical quiescent power dissipation of low-power CMOS units is

(A) 1mW. **(B)** 0.5 mW.
(C) 2 nW. **(D)** 50 nW.

h. The access times of MOSRAMS is approximately

(A) 35 ns. **(B)** 80 ns.
(C) 400 ns. **(D)** 20 ns.

i. For which of the following flip-flops, the output is clearly defined for all combinations of two inputs.

(A) D type flip-flop. **(B)** R-S flip-flop.
(C) J-K flip-flop. **(D)** none of these.

j. Active load is used in the collector of the difference amplifier of an Op-amp:

(A) To increase the output resistance.
(B) To increase the differential gain.
(C) To handle large signals.
(D) To provide symmetry.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What are the requirements of the output stage of an OPAMP? Write the circuit of the output stage of the $\mu A741$ OPAMP. **(7)**

b. Why do you require dc level shifting in OPAMPs? What are the requirements of the level shifting stage? Write a typical circuit for measuring the input bias current of an OPAMP and explain the procedure for measurement. **(9)**

Q.3 a. What is an active filter? What is the role of the amplifier of the active filter? What are the limitations of active filters? **(9)**

b. Write the squared magnitude Butterworth response and the second order normalised Butterworth polynomial. Design a fourth order Butterworth LPF by

cascading two second order prototypes. Take the cut-off frequency as one kilohertz. **(7)**

Q.4 a. What are the advantages of switched capacitor filters? Design a switched capacitor integrator for critical frequency of 20 Hz. Assume frequency of clock as 2 KHz. Compare with an RC integrator. **(10)**

b. Find the order of a Chebyshev filter with equiripple passband and following specifications:
Passband ripple $\leq$ 2 dB;
Passband edge = 1 rad/sec;
Stopband attenuation $\geq$ 20 dB;
Stopband edge = 1.3 rad/sec. **(6)**

Q.5 a. Draw a neat sketch of a 3-bit parallel comparator ADC. What are the reference levels set up for the comparator by the reference voltage divider? Which are the components that limit the conversion time? What type of ICs are recommended for flash converters of 6-bits and UP? **(10)**

b. Briefly explain the operation of an antilog amplifier circuit that uses two OPAMPS. **(6)**

Q.6 a. Briefly explain how the speed of a transistor response can be improved by preventing the transistor from going into saturation. **(4)**

b. Comment on the switching speeds in FET devices. **(4)**

c. What are the advantages of CMOS gates? Briefly explain an NMOS two-input NAND gate. Assume that positive logic is intended. What is 'SOS' as used in IC technology? **(8)**

Q.7 a. What is TTL? Illustrate the simplest and most elemental form of a TTL gate by a sketch and explain its operation when the input to the gate is 'HIGH' and 'LOW'. What is the main reason for the speed limitation of TTL? How can this be eliminated? **(8)**

b. In what type of applications is the ECL recommended? Justify its suitability in such application. Write the circuit of a 3-input ECL OR/NOR gate and mention its features. What is its logic symbol? **(8)**

Q.8 a. Two binary numbers $A_2A_1A_0$ and $B_2B_1B_0$ $(A_0 \& B_0 : LSB's)$ are to be added. Draw the scheme of a parallel binary adder consisting of half adders and explain its operation. **(7)**

b. Explain how an S-R flip-flop can be converted into a J-K flip-flop. **(5)**

c. Briefly explain the operation of a 4-to-1 line multiplexer using AND-OR logic. **(4)**

Q.9 a. What is a programmable logic device? Illustrate by a neat sketch the configuration of AND and OR arrays for a PAL with 5 inputs, 8 programmable AND gates, and 4 fixed OR gates. **(6)**

b. List the advantages of a programmable logic device over fixed function ICs. **(4)**

c. Write the basic structure of a sequence generator using a shift register and design a sequence generator to generate the sequence 1101011. **(6)**