Code No: R05310402 **Set No. 2**

III B.Tech I Semester Regular Examinations, November 2007
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.
   (b) Analyze the fall time of CMOS inverter output with $R_L = 100\Omega, V_L = 2.5V$ *and* $C_L = 10PF$. Assume V_L as stable state voltage. [8+8]

2. (a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.
   (b) Explain sinking current and sourcing current of TTL output. Which of the above parameters decide the fan-out and how? [8+8]

3. (a) Write a VHDL Entity and Architecture for the following function?

$$F(x) = a \oplus b \oplus c$$

   Also draw the relevant logic diagram.
   (b) Explain the use of Packages Give the syntax and structure of a package in VHDL [8+8]

4. Design the logic circuit and write a data-flow style VHDL program for the following functions.
   (a) $F(X) = \Sigma_{A,B,C,D}\,(0, 2, 5, 7, 8, 10, 13, 15) + d\,(1, 6, 11)$
   (b) $F(Y) = \Pi_{A,B,C,D}\,(1, 4, 5, 7, 9, 11, 12, 13, 15))$ [8+8]

5. With the help of logic diagram explain 74×157 multiplexer? Write the data flow style VHDL program for this IC? [16]

6. Design a 24-bit comparator circuit using 74×682 ICs and discuss the functionality of the circuit. Also implement VHDL source code in data flow style. [16]

7. (a) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table.
   (b) Design a Modulo-12 ripple counter using 74×74? Write a VHDL program for this logic using data flow style. [8+8]

8. (a) Discuss how PROM, EPROM and EEPROM technologies differ from each other.

(b) With the help of timing waveforms, explain read and write operations of SRAM. [8+8]

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