Code No: R05310402 **Set No. 3**

III B.Tech I Semester Regular Examinations, November 2007
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the operation of the circuit diagram.
   (b) Design a CMOS transistor circuit that has the functional behavior as

$$f(x) = \overline{(a + \overline{b})\ (b\ +\ c)(a + \overline{c})}$$

   Also draw the relevant circuit diagrams. [8+8]

2. (a) Explain the following terms with reference to TTL gate.
      i. Voltage levels for logic '1' & logic '0'
      ii. DC Noise margin
      iii. Low-state unit load
      iv. High-state fan-out
   (b) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table. [8+8]

3. Explain with an example the syntax and the function of the following VHDL statements.
   (a) Process statement
   (b) If, else and elseif statements
   (c) Case statement
   (d) Loop statement [4×4=16]

4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]

5. (a) It is necessary to identify the position of mechanical disk, when rotates with a step of 45^0. Give the necessary encoding mechanism and draw the logic circuit?
   (b) Using two 74×138 decoders design a 4 to 16 decoder. [16]

6. (a) Write a VHDL program for the circuit that counts number of Ones in a 16-bit register using structural style of modeling.
   (b) Design a 4×4 combinational multiplier and the write the necessary VHDL program data flow model. [8+8]

7. Show the logic diagram of 74×175 IC and write VHDL program for this IC in data flow style. Using this entity develop the program for 16-bit register and show the corresponding circuit also explain how the register is cleared? [16]

8. (a) Draw the basic cell structure of Dynamic RAM. What is the necessity of refresh cycle? Explain the timing requirements of refresh operation.

   (b) Discuss in detail ROM access mechanism with the help of timing waveforms. [8+8]

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