Code No: R059210202 **Set No. 2**

II B.Tech I Semester Regular Examinations, November 2007
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Prove that an RC circuit behaves as a reasonably good integrator if RC > 15T, Where T is the period of an input '$E_m \sin \omega t'$.
   (b) What is the ratio of the rise time of the three sections in cascade to the rise time of Single section of low pass RC circuit. [8+8]

2. (a) State and prove clamping -circuit theorem.
   (b) A clamping circuit and input wave form is shown in figure 2b calculate and plot to scale the steady state output [8+8]

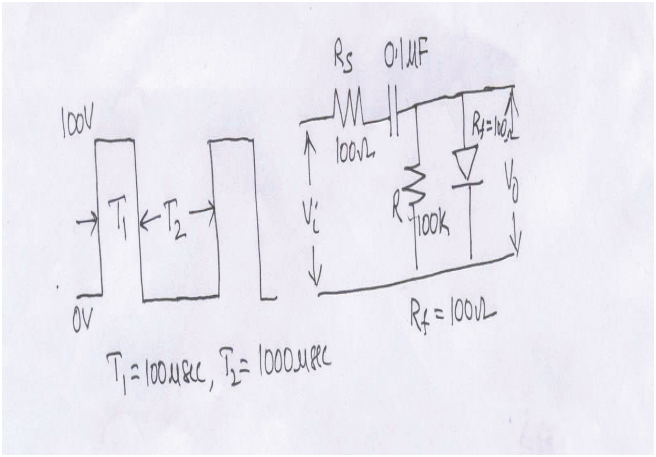

Figure 2b

3. Write Short notes on:
   (a) Diode switching times
   (b) Switching characteristics of transistors
   (c) FET as a switch. [4+8+4]

4. (a) Consider the symmetrical emitter triggering circuit of the figure 4 with Rc=3Re, R_1=2R2, and V_{CC}=6V. Indicate all the circuit voltages in the quiescent state and indicate also the voltages immediately after a 5-V positive step is applied. Assume that D3 and D4 are always in the breakdown region and that either D1 or D2 but not both in the breakdown region.

(b) Repeat part (a) for a 25-V step. What limits the maximum size of the input step? What limits the minimum size of the input step? [16]

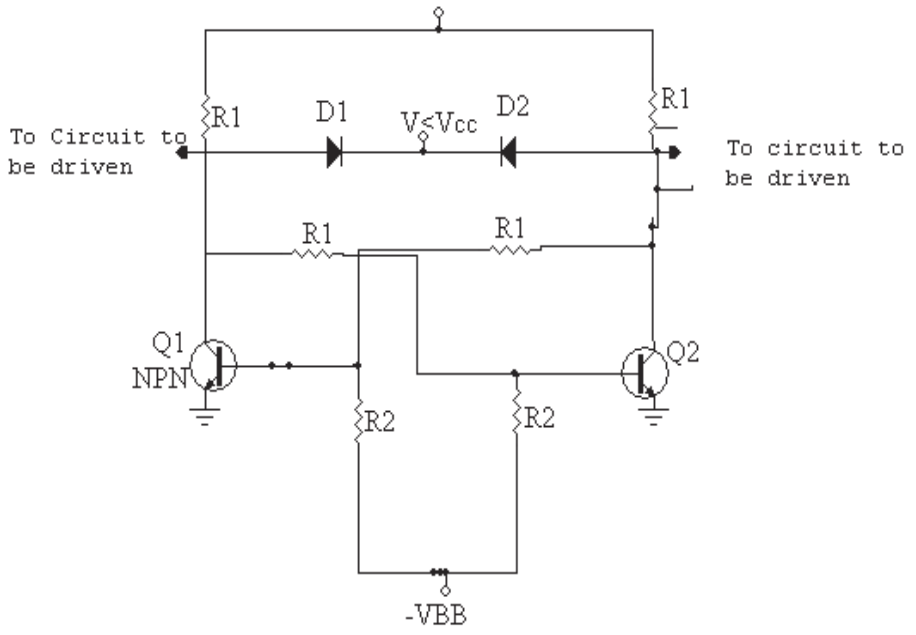

Figure 4

5. (a) Draw and clearly indicate the restoration time and flyback time on the typical waveform of a time base voltage.
   (b) Derive the relation between the slope, transmission and displacement errors
   (c) Explain how UJT is used for sweep circuit? [6+4+6]

6. (a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.
   (b) A UJT sweep operates with Vv = 3V, Vp=16V and η=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal? [8+8]

7. (a) What is sampling gate? Explain how it differ from Logic gates?
   (b) What is pedestal? How it effects the output of a sampling gates?
   (c) What are the drawbacks of two diode sampling gate? [6+6+4]

8. (a) Draw and explain the circuit diagram of integrated positive RTL NOR gate
   (b) Compare the RTL and DTL logic families in terms of Fan out, propagation delay, power dissipated per gate and noise immunity. [8+8]

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