S 9118

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Fourth Semester

Electronics and Communication Engineering

EC 242 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert the gray code number 11011 to binary.

2. What is even parity?

3. What does LS in 74LS00 indicate?

4. Define noise margin.

5. Define priority encoder.

6. Realize $S(X, Y, Z) = \Sigma(1, 2, 4, 5)$ using an appropriate decoder and an external logic gate.

7. What are the next state equations of RS and JK FFs?

8. Draw the Mealy state graph for an odd parity generator.

9. Why do races occur in asynchronous sequential circuits?

10. Define equivalence of two states in asynchronous sequential circuits.

PART B — ($5 \times 16 = 80$ marks)

11. (a) Define static, dynamic essential hazards and sequential circuits.

Or

(b) Obtain the primitive flow table for an asynchronous circuit with two inputs (T and P) and one output (Z). The output toggles when T = 1 and P input goes from 1 to 0. For all other conditions, output does not change, Assume initiallv Z = 0. (16)

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12. (a) Simplify using tabulation method.

$F(V, W, X, Y, Z) = \Sigma(4,5,6,7,9,10,14,19,26,30,31)$

Or

(b) (i) Realize XOR function using four NAND gates only. (8)

(ii) Obtain simplified POS using K–map for

$F(a, b, c, d,) = \Sigma(0,2,3,4,8,10,12,13,14)$ (8)

13. (a) (i) Explain the working of TTL Tristate gate. (12)

(ii) Write about WIRED–AND logic (4)

Or

(b) Explain the working of HTL gate and obstain its noise margin value.

14. (a) (i) Construct a 5 × 32 decoder with four 3 × 5 decoders and a 2 × 4 decoder. Use block diagrams. (10)

(ii) Write briefly about EPROM and EEPROM. (6)

Or

(b) Obtain the PLA program table with only seven product terms for a BCD to Excess–3 code converter. Also give the fuse map.

15. (a) (i) Design a counter with binary sequence 0, 2, 4, 6, 7 and repeat. Use T FFs and don't cares for unspecified states. (8)

(ii) Modify the same counter design which will lead the counter to a valid state when it lands up in an unspecified state. (8)

Or

(b) (i) Reduce the state table using implication chart method.

Present State	a	b	c	d	e	f	g
Next State X = 0	a	c	a	e	a	g	a
Next State X = 1	b	d	d	f	f	f	f
Output	0	0	0	1	1	1	1

(10)

(ii) Write about race free assignments. (6)