ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2007

DIGITAL ELECTRONIC CIRCUITS

SEMESTER – 4

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives of the following : $10 \times 1 = 10$

i) Which of the following is self-complementing code ?

a) Gray b) Excess-3

c) BCD d) Parity code

e) Hamming code.

ii) Which one is known as reflected code ?

a) Gray b) Excess-3

c) BCD d) Hamming code

e) Parity code.

iii) $(15)_{10} - (27)_{10}$ is equal to (using 2's complementing method) :

a) 01100 b) 10100

c) 00100 d) 11100

e) 01010.

iv) 2's complement of which 5-bit binary number is the same number ?

a) 11111 b) 00001

c) 01000 d) 01111

e) 10000.

v) If $\sqrt{(34)}$ is equal to 5 in a particular number system, then base of that number system is

a) 5 b) 6

c) 7 d) 8

e) 9.

vi) How many Flip-flops are required to design MOD-1024 counter ?

a) 1024 b) 102

c) 10 d) 1

e) None of these.

vii) Resolution of n-bit DAC is given by

a) $1 / (2^n - 1)$ b) $1/2^n$

c) $1/(2^n + 1)$ d) $1/2^{-n}$.

viii) To design an MOD-N Johnson Counter the number of FFs required are

a) N b) $(N - 1)$

c) 7 d) $N/2$.

ix) Race around condition occurs in a JK flip-flop when

a) $J = K = 0$ b) $J = K = 1$

c) $J = 0, K = 1$ d) $J = 1, K = 0$.

x) A memory has 16 bit address bus. The number of location in the memory are

a) 16 b) 32

c) 1024 d) 65536.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Check whether the Even parity Hamming code for 4-bit data, $(1001011)_2$ is correct or not. If not, correct the code. 4 + 1

3. Minimize the expression using *K*-Map technique :

$$Y (A, B, C, D) = ABCD + \bar{B}CD + \bar{A} \cdot \bar{B} + A + BD.$$

4. Implement the function using only one 8 × 1 MUX and *(connect only B,C,D with select lines to select the data inputs)*

$$F (A, B, C, D) = \Sigma m (0, 1, 2, 5, 9, 11, 13, 15).$$

5. Draw neat diagram of 4-bit Bi-directional shift register using mode control (M). When M is logic zero then left shift and right shift for M is logic one.

6. Design Adder/Subtractor composite unit using 4-bit binary full adder and necessary logic gates.

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions of the following. $3 \times 15 = 45$

7. a) Minimize the following expression using *K*-map and realise the simplified function using NOR gates only

$$F (A, B, C, D) = \pi M (1, 2, 3, 8, 9, 10, 11, 14) d (7, 15)$$ 3 + 3

b) Find the complement of $(735)_8$ 2

c) Draw the logic circuit diagram for a 2-to-4 decoder with one active low enable line. Assume also that all the outputs of the decoders are active low. 4

d) How do you cascade two 2-to-4 decoders to make one 3-to-8 decoder ? Draw the necessary circuit. 3

8. a) What is ROM and RAM ? What is the basic difference between EPROM and EEROM ? 5

b) A ROM is used to implement of the Boolean function :

$$F_1(A, B, C, D) = ABCD + \bar{A}\,\bar{B}\,\bar{C}\,\bar{D}$$

$$F_2(A, B, C, D) = (A + B)\ (\bar{A} + \bar{B} + \bar{C})$$

$$F_3(A, B, C, D) = \sum_m (13, 15)$$

i) What is the minimum size of ROM required ?

ii) Determine the data in each location of the ROM. 5 + 5

9. a) Draw the state table of a JK flip-flop and write down its characteristic equation.

b) Draw the circuit of Master / Slave JK flip-flop and explain the operation of the circuit.

c) What do you mean by 0's catching and 1's catching phenomena in the master / slave JK flip-flop ? 5 + 6 + 4

10. a) Describe the operation of a Flash Type A/D converter with proper circuit. 6

b) What are the advantages and disadvantages of the Flash Type A/D converter ? 3

c) Discuss the following TTL parameters briefly : 3 × 2

i) Floating input

ii) Fan-out

iii) Switching speed.

11. a) Draw the timing diagram of a MOD-10 counter where the MOD-10 counter is designed by cascading MOD-2 followed by MOD-5 counter units.

b) Design a sequential circuit that implements the following state diagram. Use all *D*-type *FF* for the design. 7 + 8