

**B.TECH DEGREE (F.T) III SEMESTER EXAMINATION IN INFORMATION
TECHNOLOGY/COMPUTER SCIENCE AND ENGINEERING, JULY 1997**

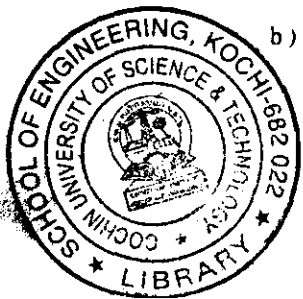
IT/CS 304 DIGITAL CIRCUITS AND LOGIC DESIGN

Time: 3 Hours

Max.marks: 100

- I a) Convert the following decimal numbers to binary and then to Octal and Hexa decimal. (6)
(i) 46 (ii) 327.89 (iii) 20.305
- b) Explain the different types of error detecting and error correcting codes. (9)
- OR
- II a) Represent the following decimal numbers in 2's complement format. (4)
(i) +3 (ii) +25 (iii) -5 (iv) -11
- b) Simplify from first principles the functions (6)
(i) $F = \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD + \overline{A}BCD + \overline{A}B\overline{C}D + AB\overline{C}D + ABCD$
(ii) $F = \overline{A}B\overline{C} + \overline{A}B\overline{D} + CD$ (5)
- III a) Implement the following switching function using NOR gates only. (7)
 $f(A, B, C, D) = \sum m(4,5,7,12,14,15) + \phi(3,8,10)$
- b) Draw the diagram for a full subtractor and explain its working. (8)
- OR
- IV a) Make a k map for the following function and realise it using NAND gates only. (7)
 $f(A, B, C, D) = AB + A\overline{C} + C + AD + A\overline{B}C + ABC$
- b) Design a BCD to excess 3 code convertor. (8)
- V a) Explain the following terms as applied to a logic family. (6)
i) Speed - power product ii) Fan-out iii) Noise margin
- b) Draw the circuit diagram of a basic 2-input NAND gate in TTL and explain its operation. (9)
- OR
- VI a) Discuss the problems encountered while a CMOS gate is used to drive N TTL gates and explain how interfacing can be done. (10)
- b) Explain tristate logic and its applications. (5)
- VII a) Explain the difference between a sequential system and a combinational system, giving examples of each. (5)
- b) Draw a logic diagram for a mod-8 Up Down counter and explain. (10)

(P.T.O)



OR

- VIII a) Explain how T and D flip-flops are constructed using J-K flip-flops. (5)
- b) Design a counter which counts through the following sequence
2-3-4-5-6-7-2,..... (10)
- IX a) Draw the circuit of a MOS dynamic RAM cell and explain its working. (5)
- b) Design a 4 line to 1 line multiplexer. (10)

OR

- X a) What is meant by PLA? What are its advantages? How does it differ from a ROM. (5)
- b) Implement the following multi-output combinational logic circuit using a 4 to 16 line decoder. (10)

$$F_1 = \sum m (1,2,4,7,8,11,12,13), \quad F_2 = \sum m (2,3,9,11)$$

$$F_3 = \sum m (10,12,13,14) \quad F_4 = \sum m (2,4,8)$$

- XI Write short notes on any 5 of the following. (5 x 5)

- 1) LSI, MSI and VLSI chips
- 2) Johnson counter
- 3) Synchronous counter
- 4) EPROM
- 5) BCD codes
- 6) Triggering of flip-flops
- 7) Sequence generator
- 8) Master-slave J-K flip-flop.
