X. (a) Realise a 32 - to - 1 line multiplexer using four 8 : 1 muxes and one 4 : 1 mux. (12)

(b) Write short note on 'EPROM'. (4)

(c) (i) How many address lines are there in the decoder of a 512 x 1 bit ROM?

(ii) How many number of NAND gates are needed in the decoder for a 1024 x 2 bit ROM? (4)

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B.Tech. Degree III Semester Examination
January 2002

IT 304 ELECTRONIC CIRCUITS AND LOGIC DESIGN

Time: 3 Hours Maximum Marks: 100

I. (a) Draw and explain the frequency response of an RC coupled amplifier. What is the role played various inter-electrode and wiring capacitors? (10)

(b) Explain the construction of a crystal oscillator. Give the expression for resonant frequency. (8)

(c) Why JFET is preferred in the design of front end of Radio Receivers? (2)

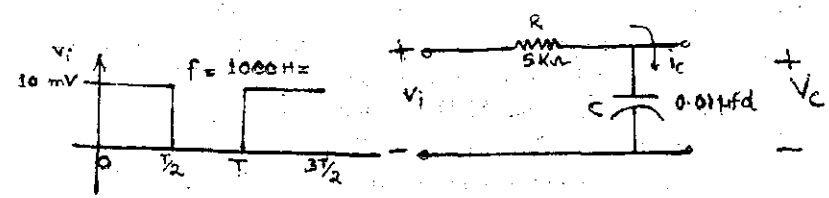
OR

II. (a) Explain the drain curves for n-channel JFET. Show the different operating regions. What is I_{DSS}, $V_{GS(off)}$, V_P? (12)

(b) Explain with necessary diagram the working of Weinbridge oscillator. (6)

(c) Specify the use of transformer coupling. (2)

III. (a) In the figure given below, the 1000Hz square wave is applied to the RC circuit. Compare the pulse width of the square wave to the time constant of the circuit. Sketch V_c (t). (10)



III. (b) Describe the working of positive voltage clamper with sinusoidal input. (6)

(c) Bringout the difference between differential gain and common-mode gain.
What is CMRR? (4)

OR

IV. (a) Explain the working of SCR using two transistor theory. Derive the condition required for turning ON the SCR. (8)

(b) Explain the function of a 2-level diode clipper with necessary input, output waveforms. (6)

(c) Determine the output voltage of a differential amplifier for input voltages of $V_{i_1} = 150\mu V$ and $V_{i_2} = 100\mu V$.
The amplifier has a differential mode gain of $A_d = 1000$ and the value of CMRR is 40dB. Why high CMRR is desirable for op-amp? (6)

V. (a) Realise a 4 bit Gray to 8421 code converter using basic gates.

Input gray code is	G_3	G_2	G_1	G_0
Output 8421 code is	W	X	Y	Z

Use the K-map for simplification. (10)

(b) Give the NOR-NOR implementation of $F = AB + \overline{B}C$. (6)

(c) Why NAND gate is called a universal building block? Illustrate. (4)

OR

VI. (a) Realise a Full adder using only NAND gates. Give the truth table for full adder. Realise the full adder using half adder and basic gates. (10)

(b) Show that AND gate in a positive logic is the same as the OR gate in a negative logic. (6)

(c) Find the canonical expansion of $X\overline{Y} + YZ + \overline{X}Z$.
Distinguish between canonical and non-canonical form. (4)

Contd.....3.

VII. (a) Explain the following terms with respect to digital ICs.
(i) Noise margin (ii) Fan out
(iii) Logic flexibility (iv) Operating speed
(v) Power dissipation (10)

(b) Specify at least two application areas where the following digital IC families are used.
(i) TTL (ii) CMOS
(iii) ECL (6)

(c) Realise a 3-bit Ring counter using JK flipflops.
Give the count sequence. (4)

OR

VIII. (a) Summarise the advantages, limitations and typical application areas of CMOS digital ICs. (8)

(b) An 8-bit ring counter uses a clock frequency of 2MHz.
(i) How long is each timing bit high?
(ii) How long does it take to cycle through all the counts? (4)

(c) Design a mod 5 synchronous counter using JK flipflops. (8)

IX. (a) Differentiate between PLA and PAL devices. (6)

(b) Design an encoder using diode matrix for the following truth table. (6)

Inputs				Outputs			
X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0
0	0	0	1	0	1	1	1
0	0	1	0	1	1	0	0
0	1	0	0	1	1	0	1
1	0	0	0	0	0	1	0

(c) Realise a 4 line-to-10 line decoder using basic gates.
Give the required truth table (8)

OR

Contd.....4.