C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
b) Show an implementation of the Equality comparator of two 2-bit vectors using a network of 2 input multiplexers.
c) Explain Parallel input Unidirectional Shift register with Load and Shift control.
d) Explain how Wired Logic can be implemented in TTL family.
e) Differentiate between MOS and Junction transistor.
f) Describe a Schottky TTL gate by giving an appropriate diagram.
g) Differentiate between behavioral and dataflow modeling in terms of Signal assignments.

(7x4)

2.

a) Design a minimal two-level gate combinational network that detects the presence of any of the six illegal groups in the 8421 code by providing a logic-1 output.
b) Realize following function with a 3 to 8 line decoder + gates.

$F1(x2,x1,x0) = \pi M(0,3,5)$
$F2(x2,x1,x0) = \pi M(2,3,4)$

c) Describe depletion and enhancement mode devices. Show the use of MOSFET as Resistor.

(6+6+6)

3.

a) Using a 4 bit binary adder, design a network to convert a decimal digit in excess-3 code into a decimal digit in 8421 codes.
b) Derive PLA program table for a combinational circuit that squares a 3-bit number. Minimize the number of product terms.

(9+9)

4.

a) Design up-down counter using J-K flip-flops.
b) What do you mean by lock-out of a counter? How do you test for the problem of lock-out of a counter? How do you eliminate this problem?
c) What is Race Around problem? How is it handled in Master-Slave J-K flip-flop?

(8+6+4)

5.

a) Design a Sequence detector which detects following binary sequence: 0 1 1 0 1 0
b) Design a sequential circuit described by the following state equations. Use JK flip-flops.

$A(t+1) = xAB + yA'C + xy$
$B(t+1) = xAC + y'BC'$
$C(t+1) = x'B + yAB'$

(9+9)

6.

a) Discuss the usage of packages & libraries and their binding in VHDL.
b) Write a VHDL code for 16 X 8 bit memory with address, data, read /write, enable inputs.

7.

a) Write a VHDL code for Universal shift register with Parallel load facility. Use any of three modeling.

b)
```
library ieee;
use ieee.std_logic_1164.all;

entity module1 is
      port( l,r,s1: in std_logic;
            q: out std_logic_vector(3 downto 0);
            s2: out std_logic);
end module1;

architecture behave of module1 is
      signal f: std_logic_vector(3 downto 0);
begin
      process(r,l)
      if(r = '1') then
            f <= "0000";
      elsif (l'event and  (l= '1') ) then
            f <= f(2 downto 0) & s1;
      end if;
      end process;

      q <= f;
      s2 <= f(3);
end behave;
```

i) Draw a black box of VHDL module for above code and discuss actions performed.

ii) Simulate the waveform of the above code.

(9+9)