S.E. Electronics / Sem III

Digital system Design - I

ws Oct Sacn- 10 70

Con. 5999–10. **GT–6213**

(3 Hours) **[Total Marks : 100**

N.B. : Question No. **1** is **compulsory**. Solve any **four** from rest **six**.

1. Answer the following questions 20

   (a) Define the following in your own words:
   - i) Fan-out of a gate
   - ii) Noise margin
   - iii) Propagation delay
   - iv) Digital multiplexing
   - v) Setup and hold times for a flip-flop

   (b) What are the advantages of an edge triggered flip-flop over a level triggered device. Explain with example.

   (c) Convert BCD numbers to excess-3 codes.

   (d) Convert to canonical forms:
   i) F(X,Y,Z) = X.Y' + X.Z
   ii)F(A,B,C) = (A+B').(A'+C')

2. (a) Obtain minimum SOP expressions for the following using K-maps, implement using universal gates:

   i) $F(W,X,Y,Z) = \Sigma m(2,3,6,7,8,9,12,13) + d(4,10,14)$ 3

   ii) $F(W,X,Y,Z) = \Sigma m(0,3,4,5,6,7,11,12,13,14,15)$ 3

   iii) $F(V,W,X,Y,Z) = \Pi M(2,3,6,7,12,13,14,15,18,19,22,23,25,27,28,29)$ 4

   (b)Show how IC 7483 , 4-bit adder, can be cascaded to add two 16-bit numbers. Explain with example. 10

3. (a) Simplify the following 5 variable Boolean expression using Quinn- McClusky tabulation algorithm: 10

   $F = \Sigma m (1,3,4,5,6,9,11,12,13,14,20,21,22,29,30,31) + d(7,23,28)$

   (b) Design a 4-bit Johnson (twisted ring) counter using flip-flops of your choice. Explain using waveforms. 10

4. (a) Design an clocked MN flip-flop using JK flip-flop. The function table of MN flip-flop is as follows: 10

M	N	Q_{n+1}
0	0	Q_n'
0	1	0
1	0	1
1	1	Q_n

   (b) Explain and draw MOD – 12 asynchronous counter using T- FF. Draw output waveforms and show where glitches occur. 10

[TURN OVER

5. (a) Show circuit implementations with minimum no. of gates in each of the following forms for the function F= X′ .Y + X.Y′ 10
   i) AND / OR
   ii) NAND / NAND
   iii) NOR / NOR
   iv) NAND / AND

   (b) Determine whether any static 0 or static 1 hazards exist in the following Boolean equation. Identify where the hazards are and what must be done to avoid them. 10
   $F(A,B,C,D) = \Sigma m(5,7,8,9,10,11,13,15)$

6. (a) Sketch the diagram of a TTL Nand gate. Explain how the gate output can be put into high impedance state. 10

   (b) Draw and explain a 16 - bit even parity checker using IC 74180 10

7. (a) Implement the following using single IC 74151 for each function and some gates (if required). 10
   $F1 = \Sigma m(0,1,3,5,7)$
   $F2 = \Sigma m(1,4,5,7,8,12,13,15)$

   (b) Show how a 74148, 8-line to 3-line encoder, can be used with a 74138, 3:8 decoder to save wires in transmitting information from point A to point B in a digital system. 10