S.E. (ETRX) Sem III (RD) 20-5-09

Digital System Design - I 3 p.m. to 6 p.m.

Con. 2824–09. **(REVISED COURSE)** **VR–3306**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions from remaining **six** questions.

1. (a) Obtain Hamming code for '1011' data for even parity. Why is Hamming code called error correcting code ? Justify. **20**
   (b) Simplify following logical expression using Boolean laws
   $f = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$
   (c) Explain race around condition in master-slave J–K f/f (flipflop).
   (d) Explain lockout condition in counter with example.

2. (a) Using k-map simplify the following function and implement it as a SOP and as a POS $f = \Sigma m (0, 4, 5, 6, 8, 12, 13, 14)$ **10**
   (b) There are four adjacent parking slot in a company. Each slot is equipped with a special sensor whose output is asserted low when car is occupying a slot, otherwise the sensor's output is high. Design and draw. Schematic for a system, which will generate a low output if and only if there are two or more than two adjacent slots vaccant. **10**

3. (a) Implement $f = \pi m(0, 1, 4, 5, 7)$ using 4 : 1 multiplexer. **10**
   (b) Using Quine McClusky method of minimization solve – **10**
   $f(A, B, C, D) = \Sigma m (0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$.

4. (a) Implement 9-bit odd parity checker circuit using IC = 74180. **10**
   (b) Explain comparator chip IC 7485. Design 12-bit comparator circuit using three '7485' IC. **10**

5. (a) Convert : **10**
   (i) SRFF TO TFF
   (ii) JKFF TO SRFF.
   (b) Design mod-10 asynchronous counter using J-K flip-flop. **10**

6. (a) Design 3-bit Up/Down synchronous counter using T-f/f. **10**
   (b) Explain working of 4-bit ring counter. Draw its timing diagram. **10**

7. (a) Draw a neat circuit diagram of 2 input TTL NAND gate and explain its operation. **10**
   (b) What is static hazards in a combinational digital circuit ? How it can be avoided ? **10**