B.E (COMPUTER & INFORMATION TECHNOLOGY) (SEM III) (REV)
EXAMINATION, OCTOBER 2006
[REVISED COURSE] DIGITAL LOGIC DESIGN AND APPLICATION

CON/4795-06. YM-5239

(3 Hours) [Total Marks : 100 5

Note : (1) Q. No. 1 is Compulsory.
(2) Answer any four questions from the remaining .
(3) All questions carry equal marks.
(4) Figures to the right indicate full mrks.
(5) assume suitable data if required.

1. (a) Convert (47.3)7 TO BCD , Excess- 3 , and Gray Code. (3)

(b) Perform the following operation using 2' s complement method (4)

(i) (246) 7 - (435)10

(ii) (45) 10 * (23) 10

© Perform the following operation with out converting into any other base. (4)

(i) (213) 4 * (22) 4

(ii) (ADD) H * (AD)H

(d) Explain in brief combinational PLD'S. (6)

(e) State Distribution Laws for simplification of Boolean equation and prove it. (3)

2. (a) Obtain Hamming Code for the data (1101). Why Hamming Code is called as Error Detecting Code (4)

(b) Given Logic Equation

$F = AB + AC + C + AD + ABC + ABC$

(i) Design K - Map for the given Equation . (4)

(ii) Express in SOP Equation. (4)

(iii) Minimise and Realise the above equation using NOR gates only. (4)

(iv)Realise the above equation in Standard POS and using NAND gates only. (4)

3.(a) Minimise the following equation using NOR gates only . (5)

$F(W,X,Y,Z) = \Pi M (1,2,3,8,9,10,11,14) * d(7,15)$

(b) Prove the follwing equation using Boolean Laws. (5)

(i) $(B+A)(C+D)(A+C)(B+D) = BC + AD$

(II) $(A . B . A)(A B B) = A \ominus B$

© what is a carry look ahead adder. design 4 bit carry look ahead adder using gates. (5)

(d)A Car manufacturing Company wants to design a logic cct. to allow the car to start only in the following condition (5)

(i) only when driver and front seat co- passenger are sitting with their seat belt on.

(ii) if no passenger is sitting and only the driver is sitting with the seat belt on.

4.(a) (i) Implement the following expression using only one 8 : 1 Mux. and few gates . (5)

$F = \Sigma m (0,1,3,4,5,7,9,10,12,13,15)$

(ii) Implement the following expression using only one 4 : 1 Mux. and few gates . (5)

$F = \Sigma m (0,1,2,3,6,7,9,10,13,15)$

(b) Using the Quine Mc Cluskey Method minimization technique simplify (10)

$F = \Sigma m (1,2,6,8,10,11,14,15) + d(5,9)$

[TURN OVER

5.(a) Draw J – K flip /flop using NAND gates only and explain RACE ARROUND CONDITION . (6)

(b)Obtain Characteristics table for S- R flip/flop , Characteristics equation , and excitation table. (6)

© Explain with neat diagram interfacing of TTL with CMOS and vice versa. (8)

6. (a) for the two functions of four variables , (10)

F (W,X,Y, Z) = Σm (5, 8, 9,12, 13)

F (W,X,Y,Z) = Σm (1,3,5,8,9,11)

Implement it with (i) PLA (ii) PAL

(b) Using Controlled Invertor Logic , design adder/subtractor cct. For 4 bits . (10)

7. (a) Explain Two i/p TTL Nor gate and draw the cct. (10)

(b) Write short notes on (any two): (10)

(i) universal Gates

(ii) ALU

(iii) Parity Generator

(iv) Self Complementing Code.
