

C1-R3: COMPUTER ORGANIZATION

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS

TOTAL MARKS:

100

(PART ONE – 40; PART TWO – 60)

PART ONE (Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)
 - 1.1 An 8-bit binary word $b_7b_6b_5b_4b_3b_2b_1b_0$ as an integer x ranges from
 - A) –128 to 128
 - B) –128 to 127
 - A) –256 to 256
 - C) None of the above
 - 1.2 In a J-K flip-flop the function $K = J'$ is used to realize
 - A) T- Flip-flop
 - B) S-R Flip-flop
 - C) D- Flip-flop
 - D) M/S J-K flip-flop
 - 1.3 One of the major difference between a combinational logic circuit such as a decoder and a storage circuit such as an RS latch is that:
 - A) The storage circuit requires a different class of gates
 - B) The storage circuit requires a clock input
 - C) The storage circuit uses feedback
 - D) The storage circuit has no propagation delay
 - 1.4 The Instruction Set Architecture of a microprocessor specifies (among other things) includes:
 - A) The address space available to the processor.
 - B) The memory addressing modes to be used by instructions.
 - C) The native data types of the microprocessor.
 - D) All of the above
 - 1.5 The Program Counter may be defined as a
 - A) Binary counter that keeps track of the number of instructions executed.
 - B) Register that stores the next instruction to be executed.
 - C) Register that stores the address of the next memory location to be written to.
 - D) Register that stores the memory address of the next instruction.

1.6 What logic circuit would you use for addressing memory?

- A) Full adder
- B) Multiplexer
- C) Decoder
- D) Direct Memory Access circuit

1.7 The logic expression for the following truth table in the form $Y = f(A, B, C)$ is

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

- A) $Y = ABC + A'B'C'$
- B) $Y = AB + AC$
- C) $Y = AB' + AC$
- D) $Y = ABC + AC$

1.8 How many memory locations are required to store the instruction LXIH, 0800H in an 8085 assembly language program?

- A) 1
- B) 2
- C) 3
- D) 4

1.9 How many select lines do an 8 input multiplexer have?

- A) 1
- B) 3
- C) 8
- D) 64

1.10 Reading and writing to the memory unit (RAM or off-processor memory) takes place via the:

- A) ALU and the register unit
- B) Memory address and memory data registers
- C) Program counter and the memory data register
- D) Input/output

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the “tear-off” sheet attached to the question paper, following instructions therein. (1 x 10)

- 2.1 The two Boolean expressions, $(A + B)$ and $(A \times B) + (A \times B) + (A \times B)$ are equivalent.
- 2.2 It is often observed that the falling edge-triggered sequential circuits such as registers are generally used in order to reduce the number of inputs required to select the desired output.
- 2.3 Machine instruction cycles vary in length, however time periods called T – states are of a given fixed length.
- 2.4 Static RAM requires every bit to be refreshed every few milliseconds.
- 2.5 Each assembly language statement is covered into equivalent machine language statement.
- 2.6 The execution time of an interpreted program is usually longer than that of a corresponding compiled program.
- 2.7 An instruction cycle is always consists of memory read operation.
- 2.8 In a Karnaugh map of four variables A, B, C and D, the term AB will cover a strip of two squares.
- 2.9 Using a Boolean formula in a “sum of products” form helps us designing a circuit with the minimum number of gates possible.
- 2.10 Logically, a three-state buffer is considered as an AND gate, except that if either of the two input lines (the “in” line and the “enable” line) are 0, then there is no voltage at all on the output line.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

X		Y	
3.1	The output of the circuit depends only on its current inputs	A.	Assembly language
3.2	Sum output of a full adder	B.	RISC
3.3	A single chip computer	C.	Cache
3.4	Operations, data movement and control	D.	UART
3.5	Universal logic gates	E.	Memory addressing instructions
3.6	Locality of reference	F.	Hamming code
3.7	Asynchronous Communication	G.	NAND and NOR
3.8	Error detecting and correcting code	H.	USART
3.9	One instruction per clock cycle	I.	Microcontroller
3.10	Direct, indirect and relative	J.	Combinational Circuit
		K.	Sequential Circuit
		L.	Logical AND
		M.	Logical XOR

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

A.	Storage	B.	Accumulator	C.	Stack
D.	Multiprocessing	E.	Multiprogramming	F.	Divide
G.	XOR	H.	Multiply	I.	32
J.	Harvard	K.	Interrupt	L.	16
M.	AND	N.	Wait	O.	I/O Mapped I/O

- 4.1 A latch is a(n) _____.
- 4.2 In a zero address instruction set design, the operands come from the _____.
- 4.3 In a fully associative cache with 32 entries of one word each, _____ tags must be matched against the memory address in parallel.
- 4.4 A NAND gate has inputs A and B. Its output is connected to the both of the inputs of another NAND gate. An equivalent gate for these two NAND gates is _____.
- 4.5 In modern computers, a computer knows through a (n) _____, when an I/O device has finished its current command and is ready for the next command.
- 4.6 In a one address instruction set design, when performing an operation like add or multiply or compare that requires two operands. One of them is the _____.
- 4.7 Booth Algorithm is used to _____ two integral numbers.
- 4.8 The number of 256 X 4 RAM chips required to construct a 2 KB cache is _____.
- 4.9 A digital computer, in which data memory is separate from instruction memory, is said to have _____ architecture.
- 4.10 _____ is a rudimentary form of parallel processing in which several programs are run at the same time on a uniprocessor.

PART TWO
(Answer any **FOUR** questions)

- 5.
- a) What is the role of an interrupt controller in a computer?
 - b) What is meant by a macro? Compare the relative merits and demerits of using macros instead of subroutines in a program.
 - c) What is a bootstrap loader and why must every computer have one? List four ways of loading a bootstrap routine into a computer.

(5+5+5)

- 6.
- a) What is the role of linker in program execution?
 - b) Convert the Boolean formula $(A + (B \times (C + D))) \times E$ to “sum of products” form, showing each step clearly.
 - c) What are the drawbacks of using pulse-triggered flip-flops in the design of synchronous circuits?

(5+5+5)

- 7.
- a) A decoder is a device that has N inputs and 2^N outputs. If the value represented by the input lines is k, then the kth output line is asserted. You are required to design a device similar to a decoder using logic gates. The device will have 2 inputs (IN 0 and IN 1) and 4 outputs (OUT 0 – OUT 3) with the condition that when the value of the input lines is k, all the lines of the output numbered 0 through k are asserted (i.e. set to 1). For example, if the value of the input lines were 2, then output lines 0, 1, and 2 would be asserted.
 - b) What is instruction cycle? How are different kinds of instructions interpreted?

(10+5)

- 8.
- a) Find out the simplified equation for the function f (a, b, c) using sum of products from the following truth table. Also show the design of the circuit using only NAND gates.

a	b	c	f
0	0	0	1
0	1	0	1
0	1	0	0
0	0	1	0
1	1	0	1
1	0	1	0
1	1	0	0
1	1	1	1

- b) What is the difference between zero-address, one-address and two-address instructions? Illustrate with the help of examples.

(10+5)

- 9.
- a) Describe the concurrency control and deadlock of an operating system.
 - b) Explain the role of flag registers in low-level program.
 - c) Differentiate between Polling and Interrupt Driven I/O.

(5+5+5)