C1-R3: COMPUTER ORGANIZATION

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.

2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS **TOTAL MARKS: 100**

(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1 x 10)

1.1 A combinational circuit that converts binary information from n coded inputs to a maximum of 2^n unique outputs is called as

A) encoder
B) decoder
C) multiplexer
D) demultiplexer

1.2 Decimal equivalent of the binary number 101001.1011 is

A) 41.0875
B) 40.6875
C) 41.6875
D) 40.0875

1.3 An operation that complements bits in A where there are corresponding 1's in B is called as

A) selective set
B) selective clear
C) selective complement
D) none of the above

1.4 The instruction increment AC

A) operates on data stored in the AC register
B) operates on the data stored in memory location AC
C) does not require explicit data
D) is not a valid instruction

1.5 Shift instructions are
A) Data manipulation instructions
B) Data transfer instructions
C) Program control instructions
D) All of the above

1.6 Parallel processing may occur
A) In the instruction stream
B) In the data stream
C) Both A) and B) above
D) None of the above

1.7 The half adder performs
A) Decimal addition operation for 2 decimal inputs
B) Binary addition operation for 2 binary inputs
C) Decimal addition operation for 2 binary inputs
D) Binary addition operation for 2 decimal inputs

1.8 Octal number system is
A) A positional system with weights 0 to 9
B) A positional system with weights 0 to 8
C) A positional system with weights 0 to 7
D) A non positional system with weights 0 to 7

1.9 Typical access time of DRAM is
A) 200ns
B) 20ns
C) 20×10^6ns
D) None of the above

1.10 The instruction DEC N informs the assembler to
A) Decrement the content of N
B) Decrement the data addressed by N
C) Convert signed decimal number to binary
D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "tear-off" sheet attached to the question paper, following instructions therein. (1 x 10)

2.1 A register is a group of NAND gates with each gate capable of storing one bit information.

2.2 Octal equivalence of the hexadecimal number AF63 is 127543.

2.3 A register transfer language uses symbolic notation to describe the micro operation.

2.4 SNA means skip next arithmetic instruction.

2.5 In implied mode, the operands are specified implicitly in the definition of the instruction.

2.6 Fixed-point numbers represent only integers.

2.7 Booths algorithm gives a procedure for dividing binary integers in signed 2's complement representation.

2.8 A polling procedure is used to identify the highest priority source by software means.

2.9 Virtual memory provides higher capacity memory.

2.10 A compiler is a simple program than an assembler.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1 x 10)

X		Y	
3.1	ROM	**A.**	asynchronous communication interface
3.2	Gray code	**B.**	location counter
3.3	ISZ	**C.**	mask programming
3.4	polish notation	**D.**	binary coded digit
3.5	BCD	**E.**	increment and skip if zero
3.6	UART	**F.**	places the operator before the operands
3.7	magnetic tape	**G.**	reflected code
3.8	strobe control	**H.**	memory reference instruction
3.9	MRI	**I.**	method of asynchronous data transfer
3.10	LC	**J.**	binary coded decimal
		K.	move register immediate
		L.	load counter
		M.	access is sequential
		N.	interrupt and store zero
		O.	places the operator after the operands

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1 x 10)

A.	magnetic tape	**B.**	collision	**C.**	algorithm
D.	control	**E.**	counter	**F.**	shift register
G.	mantissa	**H.**	decimal point	**I.**	stack
J.	interrupts	**K.**	status	**L.**	bootstrap
M.	pseudo instruction	**N.**	mnemonic	**O.**	absolute
P.	flowchart	**Q.**	register reference	**R.**	memory reference
S.	micro operation				

4.1 A register that goes through a predetermined sequence of states upon the application of input pulses is called as a(n) _____.

4.2 Floating point representation contains _____and exponent.

4.3 A(n) _____ is an elementary operation performed with data stored in registers.

4.4 _____ instructions use 16 bits to specify an operation.

4.5 _____ is a storage device that stores information in such a manner that the item stored last is the first item retrieved.

4.6 _____ occurs when an instruction cannot proceed because previous instructions did not complete certain operations.

4.7 The solution to any problem that is stated by a finite number of well-defined procedural steps is called a(n) _____.

4.8 A(n) _____ command is issued to activate the peripherals to inform it what to do.

4.9 A(n) _____ loader is stored in the ROM portion of main memory.

4.10 A(n) _____ is not a machine instruction but rather an instruction to the assembler giving information about some phase of the translation.

PART TWO

(Answer any **FOUR** questions)

5.

a) Draw the flowchart of Booth algorithm for multiplication of signed 2's complement numbers and explain it with an example.

b) Represent the following decimal numbers in a 6 bit two's complement format.
   i) +14
   ii) –20

c) Perform subtraction with the following unsigned binary numbers by taking the two's complement of the subtrahend. 11010 – 01101.

(10+2+3)

6.

a) Draw and explain a 4 bit adder–subtractor circuit.

b) Explain the various registers and their functions used in basic computer.

(6+9)

7.

a) Explain the different instruction formats used in computers.

b) Draw and explain the working of a floating- point adder pipeline.

c) Describe the different shift operations.

(5+5+5)

8.

a) With a block diagram of a DMA controller explain its role in data transfer.

b) By converting an SR Flip Flop into a JK Flip Flop, explain the basic constructional difference between them.

(10+5)

9.

a) Explain the various types of mapping procedures used by cache memory.

b) Implement the function F(a,b,c,e) = Σ(1,3,7,9,15) using a decoder with 3 inputs a, b, c and 8 active low outputs labeled 0 through 7 together with an active low enable input EN'. Use as few NAND gates as possible.

(10+5)