C1-R3: COMPUTER ORGANIZATION

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.

2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS   **TOTAL MARKS: 100**
(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. **Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "tear-off" answer sheet attached to the question paper, following instructions therein.** (1 x 10)

1.1   'Cycle Stealing' is associated with
A)   Data transfer among registers
B)   DMA
C)   Pipelining
D)   Microprogramming

1.2   The largest integer that can be represented in signed-2's complement representation using n bits is
A)   2n-1
B) 2^n
C) $2^{n-1} - 1$
D) $2^n - 1$

1.3   Using an additional NOT gate, a JK flip-flop can be converted into
A)   T flip-flop
B)   RS flip-flop
C)   Master Slave flip-flop
D)   D flip-flop

1.4   A microprocessor has a data bus with 64 lines and an address bus with 32 lines. The maximum number of bits that can be stored in this memory is
A) 32×2^{32}
B) 32×2^{64}
C) 64×2^{32}

D) 64×2^{64}

1.5   The expression 'delayed load' is used in context of
A)   Processor-printer communication
B)   Memory-monitor communication
C)   Pipelining
D)   Computer Arithmetic

1.6   Break points are used for
A)   stopping a program at a desired place
B)   manipulating the stack
C)   executing each instruction individually
D)   calling a subroutine

1.7   A truth table of n variables has _____ minterms.
A) n^2
B) $(n-1)^2$
C) 2^n
D) 2^{n-1}

1.8   Which of the following shift operations divide a signed binary number by 2?
A)   logical left shift
B)   logical right shift
C)   arithmetic left shift
D)   arithmetic right shift

1.9   The condition to detect overflow during the addition of two binary numbers is
A) C_n XOR C_{n-1}
B) C_n NOR C_{n-1}
C) C_n OR C_{n-1}
D) C_n AND C_{n-1}
        where C_i is the carry out of the ith significant bit.

1.10   Dual of $a + b \cdot c$ is
A) $(a + b) \cdot (a + c)$
B) $a \cdot (b + c)$
C) $a' \cdot (b' + c')$
D) $(a' + b') \cdot (a' + c')$

2. **Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "tear-off" sheet attached to the question paper, following instructions therein.** **(1 x 10)**

2.1   A high-level language program is converted to the executable form by the compiler itself.

2.2   A negative number has same representation in signed-magnitude, signed 1's complement and signed 2's complement forms.

2.3   In Booth's algorithm, numbers in 2's complement are multiplied along with their sign bits.

2.4   In virtual memory management, physical addresses are mapped to logical addresses.

2.5 $x + y \cdot z = (x + y) \cdot (x + z)$ is true in Boolean algebra.

2.6   An instruction pipeline operates on a stream of instructions by overlapping the phases of instruction cycle.

2.7   A race condition is not possible in combinational circuits.

2.8   Zero cannot be normalized.

2.9   In content addressable memories all the words in the memory are compared simultaneously.

2.10   Retrieving instruction from the memory is the instruction cycle.

3. **Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "tear-off" answer sheet attached to the question paper, following instructions therein.** **(1 x 10)**

X	Y	
3.1 Single Output Line	**A.**	von Neumann
3.2 Self complementing code	**B.**	Programmed Control Transfer
3.3 Indirect Address	**C.**	BSA
3.4 Stored program concept	**D.**	Multiplexer
3.5 CPU checking I/O flag	**E.**	2421
3.6 Subroutine call	**F.**	Odd function
3.7 Bracket less expression	**G.**	M[AR]
3.8 Simple instructions computer	**H.**	BCD
3.9 Zero address instructions	**I.**	Decoder
3.10 Multiple variable exclusive –OR	**J.**	Interrupt driven transfer
	K.	M[M[AR]]
	L.	Prefix
	M.	BUN
	N.	RISC
	O.	ISZ
	P.	Stack Organized Computer
	Q.	Infix
	R.	Even function
	S.	CISC

4. **Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "tear-off" answer sheet attached to the question paper, following instructions therein.** (1 x 10)

A.	AR	**B.**	First	**C.**	Adders
D.	Two's Complement	**E.**	Sequential	**F.**	Serial
G.	Stored Program	**H.**	Virtual	**I.**	IR
J.	Combinational	**K.**	Subtractor	**L.**	Second
M.	Memory mapped	**N.**	One's Complement	**O.**	Primary
P.	PC	**Q.**	Locality of reference	**R.**	Parallel
S.	ROM	**T.**	Isolated	**U.**	Magnetic tape

4.1 In two pass assembler, the address symbol table is generated in _____ pass.

4.2 An adder-subtractor single unit can be designed using full _____ and XOR gates.

4.3 A(n) _____ circuit can be described using truth table.

4.4 The carry out of the most significant bit is discarded during addition of two numbers in _____ form.

4.5 CPU register storing the address of next instruction to be executed is _____.

4.6 Having same read/write instructions for memory and I/O addresses is _____ I/O concept.

4.7 High hit ratio of cache memory is possible because of _____.

4.8 In _____ memory management, there is no need to have entire program in the primary memory.

4.9 In daisy-chaining priority method, all the devices that can request an interrupt are connected in _____.

4.10 A(n) _____ is a random access device.

PART TWO
(Answer any **FOUR** questions)

5.
a) A computer uses a memory unit with 128MB words of 64 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts – some bits to differentiate between one of the four addressing modes supported by the system, an operation code, a register code part to specify one of the 512 registers and an address part. Draw the instruction word format and indicate the number of bits in each part.
b) What disadvantage of strobe control method of data transfer does the handshaking protocol overcome and how?
c) Briefly describe the working of DMA.

(4+5+6)

6. A minority function is desired to be generated in a combinatorial circuit. The output should be 1 when the number of 1's is less than the number of 0's in the input. The output should be 0 otherwise. Design a 4 input minority function. Draw the circuit also.

(15)

7.
a) Using a stack organized computer with zero-address operation instructions, write a program to evaluate the arithmetic statement

$$X = \frac{A + B - C * (D + E)}{F - G * H}$$

b) List at least three differences between a branch, a subroutine call and an interrupt.

(9+6)

8.
a) Write a subroutine in assembly language to compare two words for equality.
b) Consider a computer with virtual memory having four frames/block and eight pages. Through diagrams show how many page faults will occur with the reference string 0, 1, 7, 2, 3, 2, 7, 1, 0, 3 if page replacement policies used are (i) First In First Out   (ii) Least Recently Used.

(7+8)

9.
a) Draw the flowchart to perform the subtraction of two numbers in signed magnitude form.
b) An instruction is stored at location 100 with its address field at location 101. The address field has the value 600. The value at location 600 is 400, at 900 is 300 and at 400 is 200. A processor register R1 contains the number 300. Evaluate the effective address and the operand if the addressing mode of instruction is
i)   indirect
ii)   direct
iii)   immediate
iv)   indexed with R1 as index register.
Also diagrammatically show the contents of the part of the memory according to the data given above.

(9+6)