C1-R3: COMPUTER ORGANIZATION

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.

2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS **TOTAL MARKS: 100**

(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1 x 10)

1.1 The minimum time delay between the initiations of two independent memory operations is called
A) Cycle time
B) Access time
C) Latency time
D) None of the above

1.2 From a given tautology, another tautology can be derived by interchanging
A) 0 and 1
B) AND and OR
C) Both A) and B)
D) Impossible to derive

1.3 Choose the incorrect statement
A) Bus is a group of information carrying wires
B) Bus does not create delay in data transfer
C) Bus can carry data or address
D) A bus can be shared by more than one device

1.4 The binary equivalent of the decimal number 0.4375 is
A) 0.0111
B) 0.1011
C) 0.1100
D) 0.1010

1.5 Which of the following logic families is well suited for high speed operation
A) TTL
B) ECL
C) MOS

D) CMOS

1.6 Bubble memories are preferable to floppy disks because
A) Of their higher transfer rate
B) Cost needed to store a bit is less
C) They consume less power
D) None of the above

1.7 The cost of storing one bit of information is minimum in case of
A) Cache
B) Register
C) RAM
D) None of the above

1.8 Pseudoinstructions are
A) Assembler Directives
B) Instructions in any program that has no corresponding machine code
C) Instructions in any program whose presence or absence will not change the output for any input
D) None of the above

1.9 A flip flop circuit can be used for
A) Counting
B) Scaling
C) Rectification
D) Demodulation

1.10 The number of address and data lines for a memory of 4 K X 16 is:
A) 10, 16
B) 11, 8
C) 12, 16
D) 12, 12

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "tear-off" sheet attached to the question paper, following instructions therein. (1 x 10)

2.1 EBCDIC code uses 7 bits to represent a character.
2.2 The speed imbalance between memory access and CPU operations is reduced by memory interleaving.
2.3 The idea of virtual memory is based on principal of locality of reference.
2.4 The XOR operator is distributive over AND operator.
2.5 In INX H instruction bus remains idle for one cycle.
2.6 Interrupt RST 5.5 is both level and edge sensitive.
2.7 In Boolean algebra $W\overline{x} + yx + Wy$ can be reduced to $W\overline{x} + yx$.
2.8 A micro-programmed control unit is faster than a hard wired control unit.
2.9 Parallel printer does not use RS-232C interface.
2.10 An astable multivibrator can be used as a flip flop.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1 x 10)

X		Y	
3.1	In a Vectored interrupt	**A.**	PUSH PSW will be used
3.2	In order to save accumulator value onto stack	**B.**	Volatile memory
3.3	Parity bit is included for	**C.**	halts for a predetermined time
3.4	Magnetic Disk is not a	**D.**	and produces code for another machine
3.5	An index register is used for	**E.**	Address modification
3.6	Cross Assembler runs on one machine	**F.**	Instruction set size is kept less
3.7	On arrival of an interrupt, the CPU	**G.**	Master/slave JK-Flip-Flop
3.8	Racing problems do not exist	**H.**	JK Flip flop
3.9	Von Neumann architecture is not a	**I.**	the branch is assigned to a fixed location in the memory
3.10	A typical characteristic of RISC machine is	**J.**	Error correction
		K.	MIMD architecture
		L.	ROM
		M.	RS Flip-flop

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1 x 10)

A.	Access time	**B.**	Operating system	**C.**	Control store
D.	Machine instruction	**E.**	Array	**F.**	Processor
G.	Microinstruction	**H.**	Direct address mode	**I.**	Register transfer language
J.	Circular shift register	**K.**	Memory buffer register	**L.**	Carry look ahead adder
M.	Decoder	**N.**	Multiplexer	**O.**	Encoder

4.1 The instruction of a micro programmed control unit is called as _____.

4.2 Vector processor can also be called as _____.

4.3 In _____ the effective address is equal to the address part of the instruction.

4.4 _____ is collection of programs that controls the operation of computer for the purpose of obtaining an efficient performance.

4.5 _____ has the capability of stopping the computer.

4.6 A ring counter is a(n) _____.

4.7 The _____ anticipates the carry in advance.

4.8 The _____ is used for storing the data bits.

4.9 The time difference between application of read signal and availability of data on data lines are called as _____.

4.10 A(n) _____ is a digital function that converts binary information from one coded form to another.

PART TWO

(Answer any **FOUR** questions)

5.

a) Consider a cache (M_1) and main memory (M_2) hierarchy with the following characteristics.

M_1: 16 K words, 50 ns access time

M_2: 1 M words, 400 ns access time

Assume eight word catch blocks and a set size of 256 words with set-associative mapping

i) Show the mapping between M_2 and M_1.

ii) Calculate the effective memory access time with a catch hit ratio of h=0.95.

b) Design a logic circuit that performs the operations of Exclusive – OR, Equivalence, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage.

(8+7)

6.

a) Consider a four variable Boolean function:

$F = \sum (0, 4, 6, 7, 8, 10, 11, 15)$,

Minimize this function using K map, and realize it using gates.

b) Why NAND gate is called a universal gate. Justify your answer.

c) Convert decimal number $(215)_{10}$ into i) binary, ii) binary coded hexadecimal, iii) BCD, and represent each converted number in the format of 12 bit register.

(5+4+6)

7.

a) What is the difference between isolated I/O and memory mapped I/O. What are the advantages and disadvantages of each?

b) A 36 bit-floating number has 8 bits plus a sign bit for the exponent. The mantissa is assumed to be a normalized fraction. Negative numbers in mantissa and exponent are in signed magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero?

c) Explain character oriented protocol used in data transmission.

(5+6+4)

8.

a) Write a macro named *ADD* which takes two arguments and returns the summation of these arguments. Call it in main program to perform the additions of:

i) 4, 8

ii) 7, 3

b) Write an assembly language program to convert a decimal number to binary number.

c) What is the use of addressing mode? Differentiate between index and base index addressing mode.

(6+4+5)

9.

a) With the help of suitable logic diagram explain the functioning of one bit ALU which is able to perform basic arithmetic and logic operations.

b) List any five data transfer instructions.

c) Explain the functioning of CD-ROM storage device.

(5+5+5)