

## C1-R3: COMPUTER ORGANIZATION

### NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

**TOTAL TIME: 3 HOURS**

**TOTAL MARKS: 100**  
**(PART ONE – 40; PART TWO – 60)**

### **PART ONE** **(Answer all the questions)**

1. **Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the “tear-off” answer sheet attached to the question paper, following instructions therein.** (1 x 10)
  - 1.1 A microprocessor has a data bus with 32 lines and address bus with 20 lines. The maximum number of bits that can be stored in this memory is
    - A)  $32 \times 2^{20}$
    - B)  $32 \times 2^{32}$
    - C)  $20 \times 2^{20}$
    - D)  $20 \times 2^{32}$
  - 1.2 Which memory is faster?
    - A) Register
    - B) Cache
    - C) RAM
    - D) Hard disk
  - 1.3 Which of the following gates are called universal gates?
    - A) AND and OR
    - B) AND and NAND
    - C) XOR and XNOR
    - D) NAND and NOR
  - 1.4 The decimal number +14 can be represented in 6 bit two's complement format as
    - A) 010010
    - B) 101110
    - C) 001110
    - D) 110010
  - 1.5 The full adder performs binary addition on
    - A) 2 binary digits
    - B) 3 binary digits
    - C) 2 decimal digits
    - D) 3 decimal digits

- 1.6 A reverse polish notation is evaluated with the help of
- A) Stack
  - B) RAM
  - C) ROM
  - D) None of the above
- 1.7 Pipeline arithmetic units are used to implement
- A) Floating point operations
  - B) Multiplication of fixed-point numbers
  - C) A) and B) both
  - D) None of the above
- 1.8 In NOR latch, race condition occurs when
- A)  $R=0, S=0$
  - B)  $R=0, S=1$
  - C)  $R=1, S=0$
  - D)  $R=1, S=1$
- 1.9 A register which can be incremented or decremented and whose primary function is point to data, is called
- A) Accumulator
  - B) Program Counter
  - C) Flat register
  - D) Index register
- 1.10 Which of the following is not arithmetic instruction?
- A) MUL
  - B) STORE
  - C) INC
  - D) NEG

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the “tear-off” sheet attached to the question paper, following instructions therein. (1 x 10)

- 2.1 Unicode uses 16 bits to represent a character.
- 2.2 The advantage of immediate addressing is to restrict the operand to a number that fits an address field.
- 2.3 Traps are synchronous procedures.
- 2.4 An Array processor is an example of SIMD.
- 2.5 The adjacent min terms in K-Map always differ by one bit.
- 2.6 The racing problem do not exists in RS flip-flop.
- 2.7 Scanner is one type of I/O device.
- 2.8 Program written using assembly language must be translated in machine language before it can be executed.
- 2.9 CD-ROM uses magnetic field to store information on its surface.
- 2.10 The bus can be shared by more than one device.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

X		Y	
3.1	Half Adder	A.	Flip-flop
3.2	Registers	B.	FIFO
3.3	Radix	C.	Postfix notation
3.4	Instruction cycle	D.	Combinational circuit
3.5	Subroutine	E.	External interrupts
3.6	Stack	F.	Multiplexers
3.7	Reverse Polish notation	G.	LIFO
3.8	Traps	H.	A set of instructions
3.9	Strobe	I.	Base of Numeral System
3.10	Hit Ratio	J.	Fetch and decode instruction
		K.	Internal interrupts
		L.	Asynchronous Data Transfer
		M.	Prefix notation
		N.	Mask programming
		O.	Cache Memory performance measurement

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

<b>A.</b>	CISC	<b>B.</b>	RISC	<b>C.</b>	Mantissa
<b>D.</b>	Truth table	<b>E.</b>	MSI	<b>F.</b>	Isolated
<b>G.</b>	ROM	<b>H.</b>	Direct address mode	<b>I.</b>	Flow chart
<b>J.</b>	Encoder	<b>K.</b>	Speed	<b>L.</b>	Flip-flop
<b>M.</b>	Locality	<b>N.</b>	RAM	<b>O.</b>	Exponent
<b>P.</b>	Register	<b>Q.</b>	Program counter	<b>R.</b>	Indirect address mode
<b>S.</b>	Accumulator	<b>T.</b>	VLSI	<b>U.</b>	Decoder

- 4.1 The cache memory works on the principle of \_\_\_\_\_.
- 4.2 In \_\_\_\_\_ the memory cells can be accessed for information transfer from any desired random location.
- 4.3 A typical characteristic of \_\_\_\_\_ machine is that its instruction set size is kept less.
- 4.4 A(n) \_\_\_\_\_ is a binary cell capable of storing one bit of information.
- 4.5 A circuit that converts from binary to decimal is called \_\_\_\_\_.
- 4.6 The input-output relationship of binary variable of each gate can be represented in tabular form by \_\_\_\_\_.
- 4.7 \_\_\_\_\_ devices contain thousands of gates within a single package.
- 4.8 A floating point number is normalized if most significant digit of the \_\_\_\_\_ is nonzero.
- 4.9 The \_\_\_\_\_ holds the address of next instruction to be read from memory after current instruction is executed.
- 4.10 In \_\_\_\_\_ the effective address is equal to the address part of instruction.

**PART TWO**  
(Answer any **FOUR** questions)

**5.**

- a) What is multiplexer? Draw diagram for 4-to-1 line multiplexer and explain role of data selector in multiplexer.
- b) Explain the function of 4 bit adder-subtractor.
- c) Specify the IEEE proposed floating point single format representation in hexadecimal for number: **-38.5**
- d) Fill the missing values in the following expression.  
 $(27)_{10} = ( \quad )_2 = ( \quad )_8 = ( \quad )_{16}$

**(5+4+3+3)**

**6.**

- a) What is difference between a direct and indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?
- b) Simplify the following Boolean function in product-of-sums form by means of four variable map. Draw the logic diagram with OR-AND gates.  
 $F(w, x, y, z) = \sum (2, 3, 4, 5, 6, 7, 11, 14, 15)$
- c) Show step by step multiplication process using Booth algorithm when the following binary numbers are multiplied.  
Assume 5-bit register hold signed number. The multiplicand is +15.  
 $(+15) \times (+13)$

**(4+5+6)**

**7.**

- a) Draw block diagram of DMA controller. Explain, how it works.
- b) List types of shift micro operations and explain circular shift micro operations.
- c) A digital computer has a memory unit of 64K x 16 and cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and the word fields of the address format?

**(6+5+4)**

**8.**

- a) Describe the concurrency control and deadlock of an operating system.
- b) What is Interrupt? Explain in brief, different types of interrupt with example.
- c) Give difference between handshaking method and strobe pulse method of asynchronous data transfer.

**(6+5+4)**

**9.**

- a) What do you mean by virtual memory? Explain concept of address space and memory space.
- b) What do you mean by forward reference problem? How assembler can solve this problem?
- c) Write an assembly program to reverse a given string.

**(5+5+5)**