Code No: R05310201 **Set No. 4**

III B.Tech I Semester Regular Examinations, November 2007
COMPUTER ORGANISATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.
   (b) Explain about daisy chain based bus arbitration. [16]
2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops. [8]
   (b) What are register transfer logic languages? Explain few RTL statement for branching with their actual functioning. [8]
3. (a) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]
   (b) How do we reduce number of microinstructions? What are micro-subroutines? [8]
4. (a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers. [8]
   (b) Multiply 10111 with 10011 with the above procedure given (a). Show all the registers content for each step. [8]
5. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]
6. (a) What is polling? Explain in detail.
   (b) What is daisy chaining? Explain. [8+8]
7. (a) What is pipeline? Explain space-time diagram for Pipeline.
   (b) Explain pipeline for floating point addition and subtraction. [8+8]
8. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those. [6]
   (b) Explain time-shared common bus Organization. [5]
   (c) Explain system bus structure for multiprocessors. [5]

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