Code No. 118(C)

B.Tech. Degree V Semester Examination in Electronics and Communication Engineering, March 1999

EC 501 MICROPROCESSORS

Time: 3 Hours *Max.Marks: 100*

I a) Explain in detail the function of the various components of a micro computer. (10)

b) The instruction code 01001111(4FH) is stored in memory location 2005H. Illustrate the data flow and list the sequence of events when the instruction code is fetched by the MPU. (10)

OR

II a) Explain the architecture of 8085 with a neat diagram. (12)

b) Briefly explain the functions of Reset, interrupt, Ready and Hold signals of 8085. (8)

III a) Give the addressing modes of the following instruction

i) LXI H, 2100 H	ii) RAR
iii) MOUA, M	iv) LDA 2000H
v) STAX D	vi) ACI57H
vi) LHLD 2050 H	viii) MOUA, B

(8)

b) Give the complete timing diagram showing all the relevant signals of the following instruction 2000 OUT 80H; (A) = FFH (12)

OR

IV a) Explain the function of the flag bits of 8085. (8)

(P.T.O)

b) Illustrate the stack contents with respect to the execution of the following instructions
[SP] = 2000; [B] = 0IH ; [C] = 02H ; [D] = 03H,
[SP] = 04H, [H] = 05H ; [L] = 06H (12)

```
PUSH  B
PUSH  D
PUSH  H
POP   D
POP   B
POP   H
```

What are the contents of B, C, D, E, H and L register after the above sequence of PUSH and POP instructions.

V a) Compare memory mapped and I/o mapped I/o schemes. (10)

b) What is bus contention ? Illustrate the situation using timing waveform of a memory interface to the CPU. (10)

OR

VI a) Explain DMA transfer. (8)

b) Interface 256 byte RAM, 1K RAM and 2K ROM to 8085 CPU. Show the memory map. (12)

VII a) Design a scheme by which the CPU gets the address of an ISR when an external device interrupts the CPU via the INTR pin. Draw the necessary hardware set up. (10)

b) Give the internal block diagram of 8259 A and explain the blocks. (10)

OR

VIII a) Write a BSR (bit . set Reset) control word subroutine to set bits PC_7 and PC_3 and reset them after a delay

Address of Port A = 80 H
" B = 81 H
" C = 82 H
Control register = 83 H (10)

Contd...3

b) Explain briefly any A/D converter and its interfacing to the 8085 CPU (10)

IX a) Explain the various registers within the 8086 CPU (8)

b) What do you meant by memory segmentation? Compare 8086 and 68000 with regard to the above. (12)

X a) Explain how a 20 bit address is obtained using 16 bit segment and offset registers in an 8086 CPU. (10)

b) What is mulliprocessing. (10)

***