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May 2007

Total No. of Questions : 09]

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J-1497[6410 B]

[2957]

B.Tech. (Semester - 5th)



PULSE AND DIGITAL SWITCHING CIRCUITS (EC - 309)

Time : 03 Hours

Maximum Marks : 60

Instruction to Candidates:

- 1) Section - A is compulsory.
- 2) Attempt any **Four** questions from Section - B.
- 3) Attempt any **Two** questions from Section - C.

Section - A

Q1)

(10 × 2 = 20)

- a) Define rise time and decay time of a wave.
- b) When does a low pass filter circuit acts as an integrator?
- c) Explain avalanche breakdown and Zener breakdown.
- d) What do you mean by regeneration comparator? Give an example.
- e) What are the three regions of operation of a transistor?
- f) What do you mean by resolving time and settling time of a circuit.
- g) What do you mean quasi stable state of a multivibrator?
- h) Why monostable multivibrator is called a gating circuit.
- i) Differentiate between compensated and uncompensated attenuator.
- j) Elaborate high frequency compensation in wide band amplifier.

Section - B

(4 × 5 = 20)

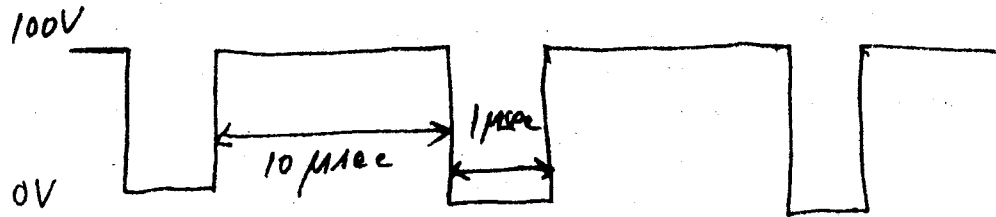
Q2) What is high pass RC circuit? Derive an expression of output voltage for square wave input and draw input-output characteristics of this circuit.

Q3) Discuss switching times of junction diode and explain the following terms with the help of diagram:

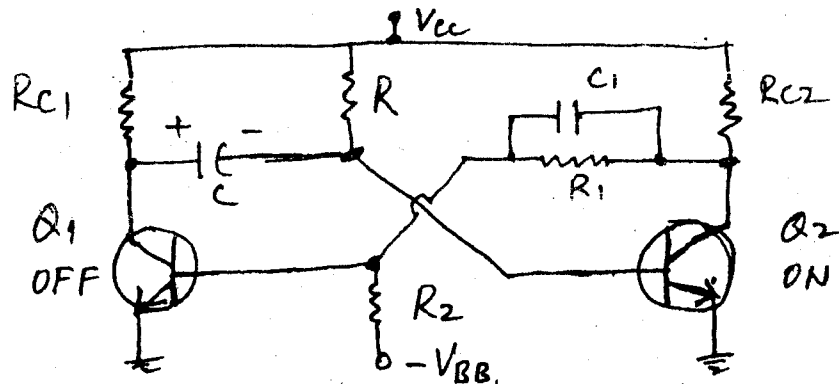
- (a) Diode forward recovery time.
- (b) Diode reverse recovery time.
- (c) Storage and transition time.

P.T.O.

Q4) The periodic waveform shown in figure below is applied to an RC integrating network whose time constant is $10 \mu\text{sec}$. Calculate the maximum and minimum values of the output voltage with respect to ground and steady state condition. Plot the output waveform for the first two cycles of the input.



Q5) Calculate the component values of a monostable multivibrator (figure below) developing an output pulse of $500 \mu\text{sec}$ duration. Assume $h_{fe}(\text{min.}) = 25$, $I_{CE}(\text{sat.}) = 5 \text{ mA}$, $V_{CC} = 10 \text{ V}$, $V_{BB} = -4 \text{ V}$, $V_{CE}(\text{sat.}) = 0.4 \text{ V}$ and $V_{BE}(\text{sat.}) = 0.8 \text{ V}$, $I_{B2}(\text{actual}) = 1.5 I_{B2}(\text{min.})$, $V_{B1}(\text{OFF}) = -1 \text{ V}$.



Q6) What is a clamping circuit theorem? Discuss a clamping circuit taking source and diode resistances into account for transient and square wave input.

Section - C

(2 × 10 = 20)

Q7) Explain the working of a astable multivibrator with the help of a neat circuit diagram and waveforms. Derive an expression for the frequency of this circuit.

- 28) (a) For a common emitter circuit, $V_{CC} = 20$ V and a collector resistance which can be either $20\text{ K}\Omega$ and $2\text{ K}\Omega$. Calculate the minimum level of base current to achieve the saturation in each case. Assuming $h_{fe}(\text{min.}) = 50$ and $V_{CE}(\text{sat.}) = 0.3$.
- (b) What do you mean by triggering? Explain symmetrically and unsymmetrically triggering through a unilateral device.
- 29) (a) Design a diode clamper circuit to restore the positive peak of 1 kHz input signal to a voltage level equal to 5 V. Assume voltage drop across diode is 0.7 V. Use a silicon diode with forward resistance, $R_f = 200\ \Omega$ and reverse resistance, $R_r = 500\text{ K}\Omega$. Assume $RC = 20\text{ T}$.
- (b) Discuss in details shunt compensation of a transistor stage in a cascade.

