SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act,1956)

Course & Branch :B.E - EIE
Title of the Paper :Digital Logic Theory and Design Max. Marks :80
Sub. Code :6C0065 Time : 3 Hours
Date :22/04/2010 Session :AN

PART - A (10 x 2 = 20)

Answer ALL the Questions

1. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (a) X – Y and (b) Y – X using 2's complements.

2. State De Morgan's theorem.

3. Compare CMOS and NMOS.

4. What are tri-state gates?

5. Give the comparison between combinational circuits and sequential circuits.

6. Difference between PROM, PLA, PAL.

7. What is race around condition?

8. Explain the procedure for state minimization.

9. Define race.

10. What are essential hazards?

PART – B (5 x 12 = 60)

Answer All the Questions

11. Simplify the Boolean function

$$F(A,B,C,D,E) = \Sigma(0,1,4,5,16,17,21,25,29)$$

(or)

12. Express the following function in sum of minterms and product of maxterm F(A,B,C,D) = B'D + A'D + BD

13. Explain TTL logic gate with a neat diagram.

(or)

14. Explain NMOS and CMOS logic gates with a neat diagram.

15. Design a combinational circuits which converts BCD to Excess-3 Code.

(or)

16. With a neat circuit diagram explain PAL.

17. A clocked sequential circuit has three states A,B,C and one input X. As long as the input X is 0, the circuit alternates between the states A and B. If the input X becomes 1 (either in state A or in State B), the circuit state C and remains in state C as long as X continues to be 1. The circuits returns to state A, if the input becomes 0 once again and from then on repeats its behaviour. Assume that the state assignments are A = 00, B = 01 and C = 10. (a) Draw the state diagram of the circuit (b) Give the state table for the circuit. (c) Draw the circuit using D-Flip-Flops.

(or)

18. Explain Synchronous Counters with neat diagram.

19. Explain Race free assignment using an example.

(or)

20. Explain pulse mode sequential circuits.