## SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)
Course \& Branch: B.E - EIE
Title of the paper: Digital Logic Theory and Design

Semester: III
Sub.Code: 6C0065 (2006/2007)
Date: 07-11-2008

Max. Marks: 80
Time: 3 Hours
Session: FN

## PART - A

$(10 \times 2=20)$
Answer All the Questions

1. Convert 1110011 into hexadecimal through octal.
2. Prove that $\mathrm{A}+{ }^{\prime} \mathrm{B}-\mathrm{A}+\mathrm{B}$, using Boolean algebra.
3. Write down fan in and fan out of a standard TTL IC.
4. Realize $\mathrm{f}=\mathrm{A}^{\prime} \mathrm{B}+\mathrm{AB}$ ' using minimum universal gates.
5. Represent a Half adder in block diagram form and also its logic implementation.
6. Define Priority Encoder.
7. What is the drawback of SR FF? How is this minimized?
8. Define Synchronous counter.
9. What is race?
10. Define equivalence of two states in Asynchronous sequential circuits.

> PART - B
$(5 \times 12=60)$
Answer All the Questions
11. Reduce the following function using K map $\mathrm{F}=\mathrm{ABC}+\mathrm{A}^{\prime} \mathrm{B}$ ' $\mathrm{C}+$ $\mathrm{ABC}+\mathrm{AB}{ }^{\prime} \mathrm{C}$ and realize using NAND gates only.
(or)
12. List out any four basic rules that are used in Boolean algebra expressions and also explain the basic laws of Boolean algebra with sample.
13. Explain the working of HTL Gate and obtain its noise margin value. (or)
14. (a) Implement the expressions
(i) $\mathrm{AB}+\mathrm{BCD}+\mathrm{EFGH}$
(ii) $(\mathrm{A}+\mathrm{B})(\mathrm{C}+\mathrm{D}+\mathrm{E})(\mathrm{F}+\mathrm{G}+\mathrm{H}+\mathrm{I})$ with logic gates
(b) Implement the following function using a quad 2 -input NOR gates. $\mathrm{F}=\left(\mathrm{A}^{\prime} \mathrm{B}+\mathrm{C}\right) . \mathrm{D}^{\prime}$
15. Obtain the PLA program table with only seven product terms for a BCD to Excess 3 code converter. Also give the fuse map.
(or)
16. (a) Realize $\mathrm{S}(\mathrm{x}, \mathrm{y}, \mathrm{z})=\Sigma(1,2,4,5)$ using an appropriate decoder and an external logic gate.
(b) Construct a $5 \times 32$ decoder with four $3 \times 5$ decoders and a $2 \times 4$ decoder use block diagrams.
17. (a) Draw a Four bit serial in serial out shift register and explain.
(b) Draw the Eight bit serial in parallel out Shift register and explain its operation.

> (or)
18. (a) Draw the logic diagram for a master slave JK FF and explain.
(b) Draw the 4 bit Johnson counter.
19. Define Sequential circuit and illustrate mixed operating mode sequential circuit model.

## (or)

20. Define the following terms.
(a) Critical race
(b) Non Critical race
(c) Hazard
(d) Flow table
(e) Static and Dynamic essential hazards.
