SATHYABAMA UNIVERSITY
(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E - EIE
Title of the paper: Digital Logic Theory and Design
Semester: III   Max. Marks: 80
Sub.Code: 6C0065   Time: 3 Hours
Date: 06-05-2008   Session: AN

PART – A   (10 x 2 = 20)
Answer All the Questions

1.   Express the following decimal numbers in 2421 and 5421 code (i) 1993

2.   State Demorgan's theorem.

3.   Give two advantages and one disadvantages of the totem pole arrangement.

4.   What is a tri-state gate?

5.   Compare Encoder and decoder.

6.   What is meant by a magnitude comparator?

7.   Draw the logic diagram of a master – slave D-flip flop using NAND gate.

8.   What do you mean by critical and Non-critical races? How can they be avoided?

9.   Why are shift registers considered to be basic memory devices?

10. How can essential hazards be eliminated?

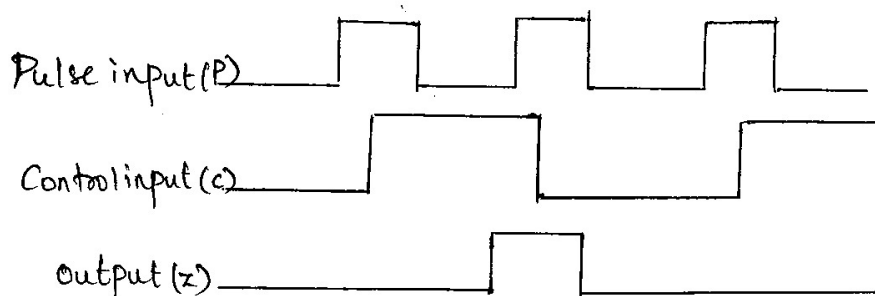PART – B   (5 x 12 = 60)
Answer All the Questions

11. Using the K-map method, Simplify the following functions into minimal sum of products
     $F(u,w,x,y,z)= \sum(0.2,5,7,9,11,13,15,16,18,21,23,25,27,29,31)$
(or)

12. Find the minimal sum of products for the Boolean expression,
     $F(a,b,c,d) = \sum(1,2,3,7,8,9,10,11,14,15)$

13. Discuss about the various parameters of TTL.

<div align="center">(or)</div>

14. (a) Draw the basic BICMOS inverter, NAND and NOR gates and explain its operation.

    (b) Draw and explain the circuit diagram of a 3-input I^2L NOR gate.

15. Explain briefly about the BCD – Seven Segment decoder.

<div align="center">(or)</div>

16. Draw and explain the basic block diagram of PLA and what are the steps used for implementing combinational circuit using PLA.

17. Design a synchronous counter with the following sequence counter
    0000   0100   0100   0110   1000   1010   1100   1110 0000.→

<div align="center">(or)</div>

18. (a) Explain the working of serial in parallel out shift register with logic diagram and waveforms.

    (b) Explain about the various applications of flip-flops.

19. Obtain a static hazard free asynchronous circuit for the following switching function.

    $$F = \sum(0,2,4,5,8,10,14)$$

<div align="center">(or)</div>

20. Design an asynchronous circuit that will output only the first pulse received whatever a control input is asserted from LOW to HIGH state. Any future pulses will be ignored.
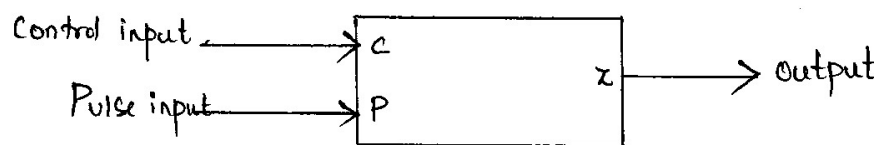
(i) Basic block diagram

(ii) Timing Diagram