SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E – CSE
Title of the paper: VLSI System Fundamentals
Semester: V Max. Marks: 80
Sub.Code: 11501(2002/2004/2005) Time: 3 Hours
Date: 24-04-2008 Session: AN

PART – A (10 x 2 = 20)

Answer All the Questions

1. Differentiate between combinational and sequential circuits.

2. Draw the circuit diagram for static CMOS inverter.

3. Differentiate between static and dynamic CMOS.

4. What is pass transistor?

5. Define “Pipelining technique”.

6. What do you mean by “dynamic sequential circuit”?

7. What is annealing?

8. What is iterative portioning?

9. What is floor planning?

10. What is power planning?

PART – B (5 x 12 = 60)

Answer All the Questions

11. Derive the expression for I – V relations for n-MOS transistor.

(or)

12. Design the model for Asynchronous state machine.

13. Discuss various techniques to reduce power consumption in CMOS gates.

(or)

14. (a) Explain DOMINO – CMOS logic with neat diagram.
    (b) Explain np-CMOS logic with neat diagram.

15. Draw the C^2MOS master-slave D flip flop. Explain its operations.

(or)

16. Write notes about "NORA – CMOS".

17. Discuss different portioning methods in detail.

(or)

18. Derive the expression for Kernighan Lin algorithm.

19. Explain the floor planning tools in detail.

(or)

20. Explain Force directed placement algorithm in detail.