SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E - CSE
Title of the paper: VLSI System Fundamentals
Semester: V — Max.Marks: 80
Sub.Code: 411501-511501-611501 — Time: 3 Hours
Date: 29-04-2009 — Session: AN

PART – A (10 x 2 = 20)

Answer All the Questions

1. What is an Excitation Table? Give an example.

2. Draw a static CMOS NAND gate.

3. What are the advantages of Pass transistor?

4. Design Y = AB + CD using dynamic CMOS.

5. What is meant by Pipelining?

6. Explain about true single phase clocked logic.

7. What are the Portioning methods available in ASIC Construction?

8. What is meant by Annealing?

9. What is meant by carry chain delay?

10. What are the goals of floor planning?

PART – B (5 x 12 = 60)

Answer All the Questions

11. Determine the Current-Voltage relationship in a MOS Device.

(or)

12. What are the Secondary effects in a MOS Device?

13. Determine the Pull-Up to Pull-down ratio for a static CMOS Inverter.

(or)

14. Explain in detail about Domino logic CMOS.

15. Explain in detail about CMOS Latch.

(or)

16. Explain in detail about Static Adder.

17. Explain in detail about Kernighan Lin Algorithm.

(or)

18. Explain in detail about Simulated Annealing.

19. Explain in detail about any one of the Floor Planning Tools.

(or)

20. Explain in detail about Force directed Placement Algorithm.