C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

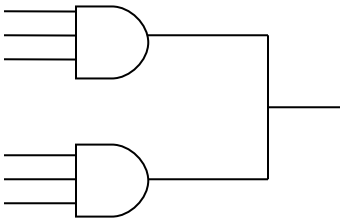
1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Why a combinational circuit is acyclic?

b) Do you allow to form a combinational gate like the following? If not why?



c) Show that a NAND gate and a NOR gate can easily be designed using a MUX.

d) Why Karnough MAP is NOT suitable for computer implementation?

e) Justify that the undefined prohibited input in R-S Latch is really impractical.

f) Distinguish between HDL and VHDL.

g) Why Booth's Algorithm is a well accepted multiplication algorithm? What is its application in Digital System Design?

(7x4)

2.

a) Simplify the following function using Karnaugh Map

$F(w,x,y,z) = \prod M(1,2,5,6,7,9,10,11,14)$

b) Describe the functionality of a PAL with block diagram.

c) What is Race Around problem? How is it handled in Master-Slave J-K flip-flop?

(6+6+6)

3.

a) Show that for n variable switching function 2^{2^n} distinct functions can be generated.

b) Show with examples that propagation delay of any combinational circuit is proportional to the depth of levels of the circuit.

(10+8)

4.

a) What are majority and parity functions?

b) Show that in a full adder circuit majority/parity functions are carry/sum outputs.

(9+9)

5.

a) Give an HDL description of Euclide's algorithm for finding greatest common divisor of two positive integers. Replace division by repeated subtraction.

b) Compare and contrast VHDL with circuit diagram.

(10+8)

6.

a) Justify the statement 'ROM' is a programmable logic device 'PLD'.

b) Give conventional and array logic symbols for OR-GATE. Explain clearly the convention.

c) Design up-down counter using J-K flip-flops?

(6+6+6)

7.

a) Explain in detail a Carry Look Ahead (CLA) adder?

b) Show that CLA outperforms ripple carry adder in general in respect of time complexity.

(8+10)