CE1-R3: ADVANCED COMPUTER ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What are the difference between scalar instructions and vector instructions? Give at least four differences.

b) A two level memory hierarchy is represented by M1 and M2. M1 has hit ratio as *h*. The access times of M1 and M2 are t1 and t2 respectively. What is the effective memory access time of this hierarchy?

c) A linear instruction pipeline having ten stages operates at 25 MHz. If one instruction is issued per clock cycle, what will be the speedup factor to execute a program of 15,000 instructions as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay? Ignore penalties due to branch instructions and out of sequence execution.

d) Draw the Illiac mesh (4x4) network. Label the nodes as N0, N1, ….., N15. List all the nodes reachable from node N0 in exactly one step.

e) State advantage and drawback of using independent request and grants in central bus arbitration system in a multiprocessor system.

f) Define Grain size. Give examples for fine, medium and coarse grains.

g) Name the two well-established concepts on which VLIW is based. Give format of the VLIW instruction.

(7x4)

2.

a) Identify dependencies among the following statements in a given program:

S1:	LOAD R1, 20H	/ R1 ← 20H /
S2:	LOAD R2, M (10H)	/ R2 ← MEMORY (10H) /
S3:	ADD R1, R2	/ R2 ← (R1) +(R2) /
S4:	STROE M (20H), R1	/ MEMORY (20H) ← R1 /
S5:	STROE M ((R2)), 20H	/ MEMORY ((R2)) ← 20H /

Explain your answer. Draw the dependency graph.

b) Explain the principle of superscalar processors with the help of timing diagram. Derive a relation for speedup of the superscalar machine over the base machine as a function of its degree, number of instructions and pipeline stages.

(9+9)

3.

a) Define (i) format of virtual and physical address and (ii) TLB and PT. How does address get translated between physical and virtual memories? Explain using TLB and PT.

b) Explain (i) the inclusion property and (ii) memory coherence requirements in a multi level memory hierarchy. Distinguish between write-through and write-back policies in maintaining the coherence in adjacent levels.

(10+8)

4.

a) Compare control-flow and data-flow computers. Give architectural details showing basic functional blocks of typical data-flow machine with brief description of each block.

b) Design a pipeline for fixed-point multiplication of 8-bit integers. Draw a schematic of the pipeline showing all line widths.

(8+10)

5.

a) What are the conflicts that are resolved in dynamic instruction scheduling based on Tomasulo's algorithm? Consider a seven stage pipeline having fetch, decode, issue, 3 executes, and write back stages. Present the schedule for the following minimum register machine code used for computing $X = Y + Z$ and $A = B \times C$. Use timing diagram for the pipeline. Add suitable wait states wherever required.

R1 ← M (*Y*); R2 ← M (*Z*);
R3 ← (R1) + (R2); M (*X*) ← R3;
R1 ←M (*B*); R2←M (*C*);
R3 ← (R1)×(R2); M (*A*) ← R3

b) Answer the following for the reservation table shown: -

	1	2	3	4
S1	X			X
S2		X		
S3			X	

i) What are the forbidden latencies?
ii) Draw the state transition diagram?
iii) List all the simple cycles and greedy cycles.
iv) Determine the optimal constant latency cycle and the minimal average latency?
v) Let the pipeline clock period be τ = 20 ns. Determine the throughput of this pipeline.

(8+10)

6.

a) Briefly describe vector instructions for register based pipeline vector machines. In what type of computations *gather, scatter and masking* instructions are used in these machines.

b) Sketch S-access memory organization for *m*-way interleaved memory. How does it work to access vector operands? Use timing diagram for your answer.

(9+9)

7.

a) What are the different buses used in multiprocessor systems? Describe each of them. With the help of these buses draw a schematic of a hierarchical bus system.

b) What are the merits and demerits of multiport memory? Show a block diagram of a system connecting processors and the multiport memories.

(9+9)