13/12/2011 BE ETRX VII (OLD)
AGJ 2nd half (e+) 46
Basics of VLSI

Con. 6581-11. (OLD COURSE) MP–6157

(3 Hours) [Total Marks : 100

NOTE:-(1) Que no 1 is compulsory.

(2) Out of remaining six questions solve any four.

(3) Each question carries 20 marks and sub-questions carry equal marks.

(4) Assume suitable data if required.

(5) Useful physical constants are given in following table.

Name	Symbol	Value	Units
Boltzmann's constant	k	1.38×10^{-23}	J/K
Dielectric constant of vacuum	ε_0	8.854×10^{-14}	F/cm
Dielectric constant of Silicon	εsi	$11.7 \times \varepsilon_0$	F/cm
Dielectric constant of SiO_2	εox	$3.97 \times \varepsilon_0$	F/cm
Intrinsic carrier concentration of silicon	ni	1.45×10^{10} at 27 °c	cm^{-3}

Que 1. (A) Draw CMOS 2 input NOR gate and explain its working.

(B) Write short notes on Latch up in CMOS.

Que 2. (A)Calculate the zero-bias threshold voltage for an NMOS Silicon-gate transistor that has well doping $= 3 \times 10^{15}$,gate doping = ND $=10^{20}$ cm^{-3} , gate- oxide thickness = 250 A^0 , and 3×10^{10} / cm^2 singly charged positive ions at the oxide-Silicon interface. Also calculate the ion- implant doses needed to achieve a threshold voltage of -1 V.

(B) Write short notes on butting and buried contacts in NMOS circuits.

Que3. Draw a circuit diagram, stick diagram of CMOS inverter and its mask layout considering lambda based design rules.

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Que4. (A) Write short notes on, " Testing of Integrated circuits".

(B) Explain Oxidation process in silicon semiconductor technology.

Que5. (A) Draw CMOS transmission gate and explain its working.

(B) Explain full scaling in VLSI.

Que6. (A) Write short notes on FET capacitance.

(B) Draw circuit diagram and stick diagram of 4:1 multiplexer using enhancement mode devices and explain its operation.

Que 7. Discuss the processing sequence of a p-well CMOS inverter with the help of cross-sectional views.