BE| ETRx | sem VII | (Rev)

Basics of VLSI

26|5|09

11am to 2pm

Con. 3255–09. **VR–4719**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining questions.

1. (a) Implement the following function using CMOS gate $F = (AB + \overline{CD})\ E$ **6**
(b) An NMOS transistor with $K = 20\ \mu A/V^2$ and $V_{TH} = 1{\cdot}5$ V is operated at $V_{GS} = 5$ V and $I_D = 100\ \mu A$. **5**
(c) Explain Ion Implantation and compare it with diffusion, clearly stating the advantages and disadvantages. **9**

2. (a) Draw the stick diagram and layout using λ-based design rule for the depletion load NMOS NOR Gate. **13**
(b) What are the various factors affecting the threshold voltage ? Explain analytically. **7**

3. (a) Explain the concept of pass transistor. Compare PMOS/NMOS and CMOS pass transistor for their merits and demerits. **10**
(b) Compare constant voltage and constant field scaling with their merits and demerits. **10**

4. (a) Explain the operation of CMOS inverter with clearly mentioning all five cases. **10**
(b) Explain the latch up in CMOS. What are the remedies to avoid the same ? **10**

5. (a) Design 4 : 1 MUX using pass transistor logic. Draw the stick diagram of same. **10**
(b) Compare Resistive, Depletion and Enhancement load inverters stating their merits and demerits. **10**

6. (a) Describe the hot electron and short channel effects in MOS devices. Also explain their effects on MOS characteristics. **10**
(b) Find the deplection layer width, red, the depletion region charge, the threshold voltage with no substrate bias and the body factor of a device with the following physical parameters. **10**

$t_{ox} = 400\ A°$, $N_a = 1{\cdot}5 \times 10^{16}/cm^3$, $N_d = 10^{18}/cm^3$.
$N_{ss} = 5 \times 10^{10}/cm^3$, $\epsilon_{si} = 1{\cdot}035 \times 10^{-12}$ F/cm
$\epsilon_{ox} = 0{\cdot}345 \times 10^{-12}$ F/cm.

7. Write short note on any **three** :– **20**
(a) VHDL in Design of IC
(b) Butting and Burried contacts in VLSI
(c) The design verification methods
(d) Custom and semicustom design methods.