VII. Rev/ ETRX / Babics VIST

Con. 2992-07.

ton

## (REVISED COURSE)

(3 Hours)

[Total Marks: 100

- N.B.(1) Question No. 1 is compulsory.
  - (2) Attempt any four questions out of remaining six questions.
  - (3) Assume suitable data, wherever required.
- (a) The segregation coefficient of oxygen is 0.25. Find the concentration of oxygen 6 in the silicon ingot at a fraction solidified of 0.3. The concentration of oxygen in the silicon at the top of the crystal is 12.5 x 10<sup>17</sup> atoms/cm<sup>3</sup> at fraction solidified of 0.1.
  - (b) Implement the following function using CMOS gate.  $F = (A + B + C)\overline{D}E$
  - (c) Describe the hot electron effect and short channel effect in MOS devices and explain 8 their effect on characteristic of MOSFET.
- 2. (a) What are the factors controlling the threshold voltage? Explain analytically (required 10 mathematical expressions). How threshold voltage is related with flatband voltage?
  - (b) Calculate the threshold voltage  $V_{TO}$  at  $V_{SB} = 0$ ,  $Q_{SO}$ ,  $C_{OX}$  for a poly gate n-channel, 10 MOS transistor.  $N_A = 10^{16}/\text{cm}^3$ . (Substrate doping),  $N_D = 2 \times 10^{20}/\text{cm}^3$  (polysilicon gate doping) ;  $t_{ox} = 500 \text{ A}^\circ$  and oxide interface fixed charge density  $N_{OX} = 4 \times 10^{10}/\text{cm}^2$ .

(Given  $n_i = 1.45 \times 10^{10}/\text{cm}^3$ ,  $\epsilon_{si} = 11.7 \times 8.854 \times 10^{-14} \text{ F/cm}$ ,  $\epsilon_{ox} = 3.97 \times 8.854 \times 10^{-14} \text{ F/cm}$ )

- (a) Explain the concept of pass transistor logic useful to implement logic function clearly 10 explain the limitations of PMOS/NMOS pass transistors. Also explain how it can be taken care of.
  - (b) Compare constant voltage and constant field scaling with clearly stating their merits 10 and demerits.
- Draw the stick diagram and layout using λ based rule for NMOS depletion load two 20 input NAND and two I/P NOR gate. Use proper color coding and aspect ratio.
- CMOS inverter is to be far licated with p-well process. Discuss various steps involved 20 in fabrication. Sketch the masking steps in cross-sectional view giving mask sequence and color of Mask to be used. Clearly mention the number of Mask required in complete process.
- (a) Explain the operation of CMOS inverter with clearly mentioning five cases given 10 below :

(i)  $V_{in} < V_{TO, n}$ (ii)  $V_{in} = V_{IL}$  (iv)  $V_{in} = V_{IH}$ (v)  $V_{in} > V_{DD} + V_{TO}$ , P

(iii)  $V_{in} = (inverter threshold)$ 

- (b) Compare Resistive load, Deplection load and Enhancement load inverters. Write 10 their merits and demerits.
- 7. Write detailed notes on any three :--
  - (a) Electron beam lithography
  - (b) VHDL in VLSI Design
  - (c) Custom and Semicustoms design methods
  - (d) Butting and burried contacts in VLSI
  - (e) CMOS latchup and protection circuits.

20

29/05/04

6

ND-920