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BSNL TTA EXAM MICRO PROCESSER

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1. A 32-bit processor has

(a) 32 registers

(b) 32 I/O devices

(c) 32 Mb of RAM

(d) a 32-bit bus or 32-bit registers

2. Clock speed is measured in

(a) bits per second

(b) Hertz

(c) bytes

(d) baud

3. A 20-bit address bus allows access to a memory of capacity

(a) 1 MB

(b) 2 MB

(c) 4 MB

(d) 8 MB

4. A microprocessor contains

(a) most of RAM

(b) most of ROM

(c) peripheral drivers

(d) most of the control and arithmetic logic functions of computer

5. Which of the following is NOT a type of processor?

(a) PowerPC

(b) Motorola 8086

(c) Motorola 68000

(d) Intel Pentium

6. If interrupt arrives on the three lines INTR, RTS 6.5 and RTS 7.5, which of them will the 8085 processor acknowledge?

(a) INTR

(b) RTS 6.5

(c) RTS 7.5

7. The Intel 8086 processor is

(a) 8-bit

(b) 16-bit

(c) 32-bit

(d) 64-bit

8. An assembly language instruction

(a) always has a label

(b) always takes at least one operand

(c) always has an operation field

(d) always modifies the status register

9. An interrupt instruction

(a) causes an unconditional transfer of control

(b) causes a conditional transfer of control

(c) modifies the status register

(d) is an I/O instruction

10. Programs are written in assembly language because they

(a) run faster than High-level language

(b) are portable

(c) easier to write than machine code programs

(d) they allow the programmer access to registers or instructions that are not usually provided by a High-level language

11. Given that the subprogram putc displays the character in al, the effect of the following instruction is -

mov al, 'c'

sub al, 2

call putc

(a) display 2

(b) display 'c'

(c) display 'a'

(d) display a blank

12. The result of mov al, 65 is to store

(a) store 0100 0010 in al

(b) store 42H in al

(c) store 40H in al

(d) store 0100 0001 in al

13. Microprocessor is also often called a

(a) Chip

(b) Resistor

(c) Capacitor

(d) Transistor

14. A microprocessor's program counter has

(a) the digital value of the data

(b) the address of an instruction

(c) the address of data

15. Which of the following is a math co-processor?

(a) 8085

(b) 8086

(c) 8087

(d) 8088

16. Interrupts are classified as

(a) Hardware interrupts

(b) Software interrupts

(c) Hardware interrupts and Software interrupts

(d) none of the above

17. The system bus is made up of

(a) data bus

(b) data bus and address bus

(c) data bus and control bus

(d) data bus, control bus and address bus

18. The memory address register is used to store -

(a) data to be transferred to memory

(b) data that has been transferred from memory

(c) the address of a memory location

(d) an instruction that has been transferred from memory

19. When an interrupt occurs, the processor completes the current _____ before jumping to the interrupt service subroutine

(a) microinstruction it is executing

(b) instruction it is executing

(c) macro it is executing

(d) subroutine it is executing

20. A microprocessor is a processor with a reduced

(a) instruction set

(b) power requirement

(c) MIPS performance

(d) none of the above

21. A scheme in which the address specifies which memory word contains the address of the operand, is called

(a) Immediate addressing

(b) Based addressing

(c) Direct addressing

(d) Indirect addressing

22. Processor gets the address of the next instruction to be processed from

(a) Instruction register

(b) Instruction counter

(c) Program counter

(d) Program register

23. Fetch operations are not required in

(a) Immediate addressing

(b) Register addressing

(c) Direct addressing

(d) Indirect addressing

24. What is meant by Maskable interrupts?

(a) An interrupt that can be turned off by the programmer.

(b) An interrupt that cannot be turned off by the programmer.

(c) An interrupt that can be turned off by the system.

(d) An interrupt that cannot be turned off by the system.

25. Which interrupts are generally used for critical events such as Power failure, Emergency, Shut off etc.?

(a) Maskable interrupts

(b) Non-Maskable interrupts

(c) none of the above

26. Which microprocessor accepts the program written for 8086 without any changes?

(a) 8085

(b) 8087

(c) 8088

27. How many memory locations are required to store the instruction LXI H, 0800H in an 8085 assembly language program?

(a) 1

(b) 2

(c) 3

(d) 4

28. How many memory fetches (including instruction fetch) are required to execute the instruction LXI H, 0800H in an 8085 assembly language program?

(a) 1

(b) 2

(c) 3

(d) 4

29. MPU stands for

(a) Multi-Processing Unit

(b) Micro-Processing Unit

(c) Mega-Processing Unit

(d) Major-Processing Unit

30. Which of the following is not possible by a microprocessor?

(a) Reading from Memory

(b) Writing into Memory

(c) Reading from Input port

(d) Writing into Input port

31. In which microprocessor does the concept of pipeline first introduced?

(a) 8086

(b) 80286

(c) 80386

(d) 80486

32. LSI stands for -

(a) Large Size Instruction

(b) Large Scale Instruction

(c) Large Size Integration

(d) Large Scale Integration

33. Which of the following is true about pseudo code?

(a) A machine language

(b) An assembly language

(c) A high level language

(d) none of the above

34. The macro processor must perform

(a) recognize macro definitions and macro calls

(b) save the macro definitions

(c) expand macro calls and substitutes arguments

(d) all of the above

35. A 32 bit microprocessor has the word length equal to

(a) 1 byte

(b) 2 byte

(c) 4 byte

(d) 8 byte

36. The TRAP interrupts mechanism of the 8085 microprocessor

(a) execute an instruction supplied by an external device through the INTA signal

(b) execute an instruction from memory location 20H

(c) executes a NOP

(d) none of the above

37. What are the states of the Auxiliary carry (AC) and Carry flag (CY) after executing the following 8085 program?

MVI H, 5DH

MVI L, 6BH

MOV A, H

ADD L

(a) AC=0 and CY=0

(b) AC=1 and CY=1

(c) AC=1 and CY=0

(d) AC=0 and CY=1

38. Contents of register A after the execution of the following 8085 microprocessor program is

MVI A, 55H

MVI C, 25H

ADD C

DAA

(a) 7AH

(b) 80H

(c) 50H

(d) 22H

39. Which of the following is a 16-bit micro processor?

(a) Motorola 6800

(b) Intel 8085

(c) Intel 8086

(d) Zilo 80

40. The Intel Pentium Pro microprocessor uses 36 address lines to access memory. What is the maximum memory that it can support, in gigabytes?

(a) 16

(b) 32

(c) 64

(d) 128

41. Out of the following which is not the flag in 8085 microprocessor

(a) Counter flag

(b) Carry flag

(c) Zero flag

(d) Parity flag

42. What is a basic element of Memory?

(a) Transistor

(b) Flip-flop

(c) Gate

(d) none of the above

43. Which group of instructions do not affect the flags?

(a) Arithmetic operations

(b) Logic operations

(c) Data transfer operations

(d) Branch operations

44. DMA stands for

(a) Direct Memory Allocation

(b) Distinct Memory Allocation

(c) Direct Memory Access

(d) Distinct Memory Access

45. In RST interrupts, RST stands for

(a) Repeat Start Test

(b) Restart

(c) Start

46. Which interrupt has the highest priority?

(a) TRAP

(b) RST 6

(c) RST 6.5

(d) INTR

47. In 8085 microprocessor with memory mapped I/O

(a) I/O device have 8-bit addresses.

(b) I/O devices are accessed using IN and OUT instructions.

(c) arithmetic and logic operations can be directly performed with the I/O data.

(d) there can be a max of 256 input devices and 256 output devices.

48. A microprocessor -

(a) reads instructions from memory

(b) communicates with I/O devices

(c) controls the timing of information flow

(d) all of the above

49. An instruction consists of

(a) Data and Address

(b) Register and Memory

(c) Opcode and Operand

(d) Input and Output

50. If the 8085 adds 87H and 79 H, which of the following flags will become 1

(a) Zero flag and Auxiliary Carry flag

(b) Zero flag and Carry flag

(c) Carry flag and Auxiliary Carry flag

(d) none of the above