

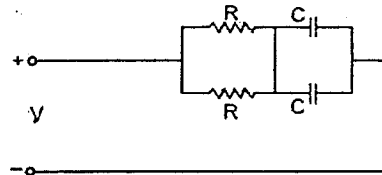
1 With fixed value capacitor C and variable voltage V across it, the energy stored in the capacitor is

- a) CV^2 b) $0.5 CV^2$ c) $2 CV^2$ d) CV

2 A dc voltage V is applied to a series RL circuit. The steady state current is

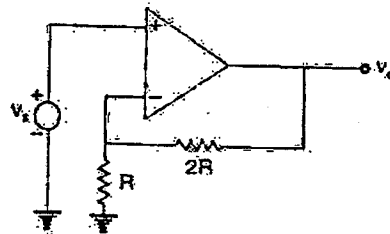
- a) V/R b) V/L c) $\frac{V}{\sqrt{R^2 + L^2}}$ d) Zero

3 The time-constant of the network shown in the figure is



- a) CR b) $2 CR$ c) $\frac{CR}{4}$ d) $\frac{CR}{2}$

4 In the ideal Op-amp circuit shown, V_o is

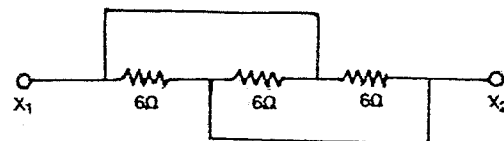


- a) $2 V_s$ b) $-2 V_s$ c) $3 V_s$ d) $-3 V_s$

5 If the unit step response of a system is a unit impulse function, then the transfer function of such a system will be

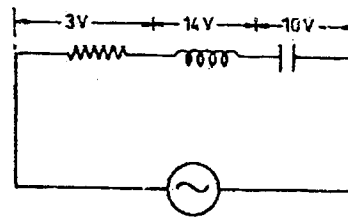
- a) 1 b) $\frac{1}{s}$ c) s d) $\frac{1}{s^2}$

6 Three resistors of 6Ω each are connected as shown in the following fig. The equivalent resistance between X_1 and X_2 is

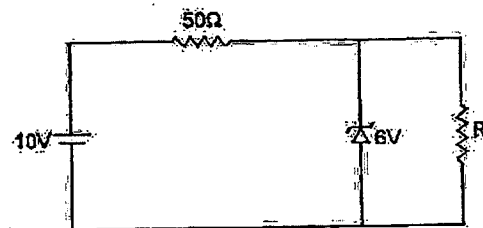


- a) 2Ω b) 4Ω c) 8Ω d) 12Ω

- 7 The source in the circuit shown is a sinusoidal source. The supply voltages across various elements are marked in the figure. The input voltage is

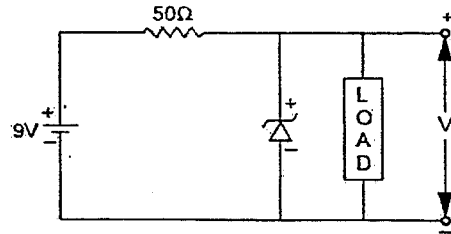


- a) 10 V b) 5 V c) 27 V d) 24 V
- 8 Laplace transform of $e^{-at} f(t)$ is
- a) $F(s)e^{-at}$ b) $F(s-a)$ c) $F(s+a)$ d) $\frac{F(s)}{s} + a$
- 9 $\cos\theta$ Can be represented by
- a) $\frac{e^{+i\theta} - e^{-i\theta}}{2}$ b) $\frac{e^{i\theta} - e^{-i\theta}}{2i}$ c) $\frac{e^{j\theta} + e^{-i\theta}}{2}$ d) $\frac{e^{i\theta} + e^{-i\theta}}{2i}$
- 10 Of the following transfer function of second order linear time-invariant systems, the underdamped system is represented by
- a) $H(S) = \frac{1}{S^2 + 4S + 4}$ b) $H(S) = \frac{1}{S^2 + 5S + 4}$
- c) $H(S) = \frac{1}{S^2 + 4.5S + 4}$ d) $H(S) = \frac{1}{S^2 + 3S + 4}$
- 11 A differential amplifier has a differential gain of 20,000. CMRR = 80 dB. The common mode gain is given by
- a) 2 b) 1 c) $\frac{1}{2}$ d) 0
- 12 Two bulbs marked 200 watt – 250 volts and 100 watt-250 volts are joined in series to 250 volt supply. Power consumed in circuits is
- a) 33 watt b) 67 watt c) 100 watt d) 300 watt
- 13 The 6 V zener diode shown in the figure, has zero zener resistance and a knee current of 5mA. The minimum value of R so that the voltage across it does not fall below 6 V is

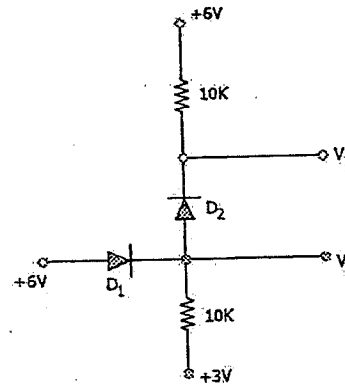


- a) 1.2 k ohms b) 80 ohms c) 50 ohms d) 0 ohms

- 14 A zener diode in the circuit shown in the figure below, has a knee current of 5mA, and a maximum allowed power dissipation of 330 mW. What are the minimum and maximum load currents that can be drawn safely from the circuit, keeping the output voltage V_0 at 6V ?

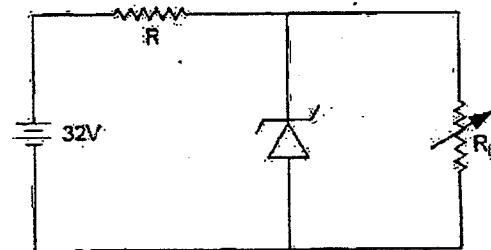


- a) 0 mA, 180 mA
 b) 5 mA, 110 mA
 c) 10 mA, 55 mA
 d) 60 mA, 180 mA
- 15 The voltages at V_1 and V_2 of the arrangement shown in the figure will be respectively



- a) 6 V and 5.4 V
 b) 5.4 V and 6 V
 c) 3 V and 5.4 V
 d) 6 V and 3 V

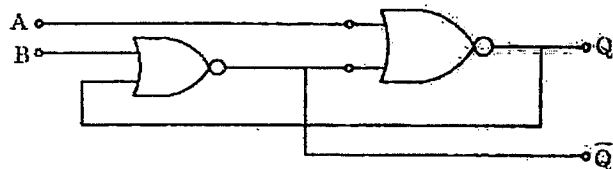
- 16 A 24 V, 600 mW, Zener diode is to be used for providing a 24 V stabilized supply to a variable load. Assume that for proper Zener action, a minimum of 10 mA must flow through the Zener. If the input voltage is 32 V, what would be the value of R and the maximum load current ?



- a) 320 Ω , 10 mA
 b) 400 Ω , 15 mA
 c) 400 Ω , 10 mA
 d) 320 Ω , 15 mA
- 17 A half – adder can be constructed using two 2-input logic gates. One of them is an AND-gate, the other is
- a) OR b) NAND c) NOR d) EX-OR

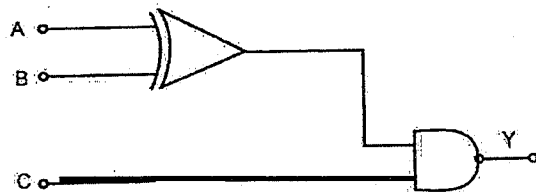
- 18 For one of the following conditions, clocked J-K flip-flop can be used as DIVIDE BY 2 circuit where the pulse train to be divided is applied at clock input.
- $J = 1, K = 1$ and the flip-flop should have active HIGH inputs
 - $J = 1, K = 1$ and the flip-flop should have active LOW inputs
 - $J = 0, K = 0$ and the flip-flop should have active HIGH inputs
 - $J = 1, K = 1$ and the flip-flop should be a negative edge triggered one
- 19 Number of comparators needed to build a 6-bit simultaneous A/D converter is
- 63
 - 64
 - 7
 - 6
- 20 The A/D converter used in a digital voltmeter could be (1) successive approximation type (2) Flash converter type (3) Dual slope converter type. The correct sequence in the increasing order of their conversion time taken is
- 1,2,3
 - 2,1,3
 - 3,2,1
 - 3,1,2

- 21 The circuit is a



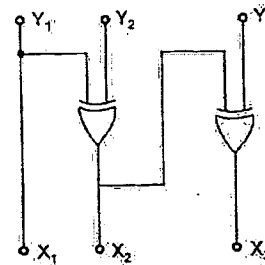
- Monostable MV
 - Astable MV
 - Adder
 - SR FF
- 22 Which of the following binary number is equal to octal number 66.3
- 101101.100
 - 1101111.111
 - 111111.1111
 - 110110.011

- 23 The Boolean expression for the output of the logic circuit shown in the figure is



- $Y = AB + \overline{AB} + C$
 - $Y = \overline{A} \overline{B} + AB + \overline{C}$
 - $Y = A \overline{B} + \overline{A} B + C$
 - $Y = AB + \overline{A} B + \overline{C}$
- 24 For the identity $AB + \overline{A}C + BC = AB + \overline{A}C$, the dual form is
- $(A+B) (\overline{A}+C)(B+C) = (A+B) (\overline{A}+C)$
 - $(\overline{A} + \overline{B}) (\overline{A} + \overline{C}) (\overline{B} + \overline{C}) = (\overline{A} + \overline{B}) (A + \overline{C})$
 - $(A+B) (\overline{A}+C) (B+C) = (\overline{A} + \overline{B}) (A + \overline{C})$
 - $\overline{A} \overline{B} + A \overline{C} + \overline{B} \overline{C} = \overline{A} \overline{B} + A \overline{C}$

25 The logic circuit given below converts a binary code $Y_1Y_2Y_3$ into



- a) Excess -3 code
- b) Gray code
- c) BCD code
- d) Hamming code

26 A 4-bit presetable UP counter has preset input 0101. The preset operation takes place as soon as the counter reaches 1111. The modulus of the counter is

- a) 5
- b) 10
- c) 11
- d) 15

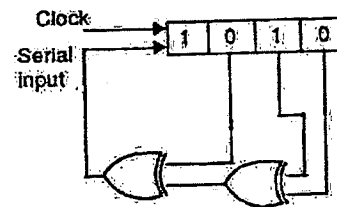
27 A 4-bit synchronous counter uses flip-flops with propagation delay time of 25 ns each. The maximum possible time required for change of state will be

- a) 25 ns
- b) 50 ns
- c) 75 ns
- d) 100 ns

28 If a counter having 10 FFs is initially at 0, what count will it hold after 2060 Pulses

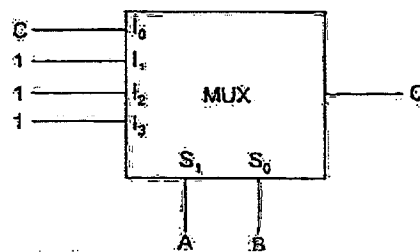
- a) 000 000 1100
- b) 000 001 1100
- c) 000 001 1000
- d) 000 000 1110

29 The shift register shown in the given figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register become 1010 again?



- a) 3
- b) 7
- c) 11
- d) 15

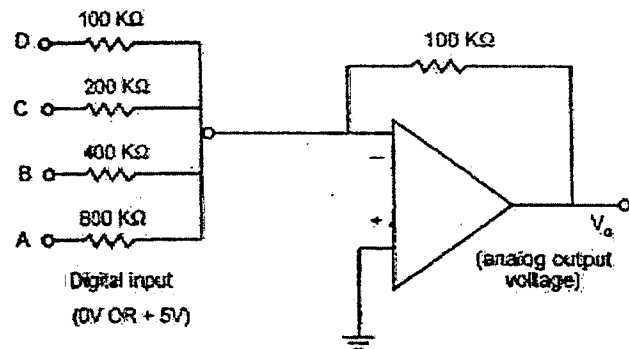
30 The combinational logic circuit shown in the given figure has an output Q which is



- a) ABC
- b) A+B+C
- c) $A \oplus B \oplus C$
- d) $A \cdot B + C$

- 31 A sample-and-hold (S/H) circuit, having a holding capacitor of 0.1nF , is used at the input of an ADC (analog-to-digital converter). The conversion time of the ADC is $1\ \mu\text{sec}$, and during this time, the capacitor should not lose more than 0.5% of the charge put across it during the sampling time. The maximum value of the input signal to the S/H circuit is 5V . The leakage current of the S/H circuit should be less than
- a) 2.5mA b) $0.25\ \text{mA}$ c) $25.0\ \mu\text{A}$ d) $2.5\ \mu\text{A}$

- 32 Determine the output voltage of a network shown in figure if the digital input is 1011



- a) $-3.875\ \text{V}$ b) $-4.875\ \text{V}$ c) $-5.875\ \text{V}$ d) $-6.875\ \text{V}$

- 33 A memory system of size 16K bytes is required to be designed using memory chips, which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is
- a) 2 b) 4 c) 8 d) 16

- 34 In time division multiplexing

- a) Time is doubled between bits of a byte
 b) Time slicing at CPU level takes place
 c) Total time available in the channel is divided between several users and each users is allotted a time slice.
 d) None of the above

- 35 When a program is being executed in an 8085 microprocessor, its Program Counter contains

- a) The number of instructions in the current program that have already been executed
 b) The total number of instructions in the program being executed
 c) The memory address of the instruction that is being currently executed
 d) The memory address of the instruction that is to be executed next

- 36 The sum S of A and B in a half Adder can be implemented by using K NAND gates. The value of K is

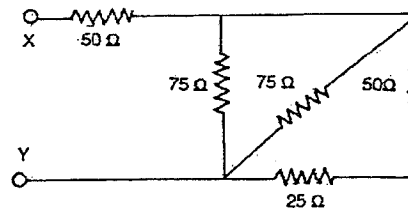
- a) 3 b) 4 c) 5 d) None of these

- 37 VSWR of a transmission line is always

- a) Less than unity b) Greater than unity
 c) Zero d) infinity

- 50 In a band limited channel higher bit rate can be transmitted with
 a) BPSK b) QPSK c) FM d) FSK
- 51 In a transmission line terminated with a load equal to the characteristic impedance, the reflection coefficient is
 a) Zero b) +1 c) -1 d) Infinity
- 52 Poynting vector $P = E \times H$ has the unit
 a) Watts/metre² b) Watts/metre c) Watts-metre d) Watts-metre²
- 53 If 1 watt of RF power is fed to a directional coupler having 30dB coupling, the power available at the coupled port is
 a) $\frac{1}{30}$ w b) $\frac{1}{10}$ w c) $\frac{1}{100}$ w d) $\frac{1}{1000}$ w
- 54 The following demodulator scheme requires least $\frac{E_b}{N_0}$
 a) BPSK b) FSK c) ASK d) QAM
- 55 The channel capacity under the Gaussian noise environment for a discrete memoryless channel with a bandwidth of 4 MHz and SNR of 31 is
 a) 20 Mbps b) 4 Mbps c) 8 Kbps d) 4 kbps
- 56 Satellite channel can be attributed
 a) Only bandwidth limited b) Only power limited
 c) Both bandwidth & power limited d) None of the above
- 57 A unit vector perpendicular to the vectors $\vec{a} = 2i - 3j + k$ and $\vec{b} = i + j - 2k$, is
 a) $\frac{1}{\sqrt{3}}(-i + j + k)$ b) $\frac{1}{\sqrt{3}}(i + j - k)$
 c) $\frac{1}{\sqrt{3}}(i + j + k)$ d) $(i + j + k)$
- 58 The region of the z plane for which $\left| \frac{z-a}{z+a} \right| = 1$ ($\text{Re } a \neq 0$) is
 a) x-axis b) y-axis
 c) The straight line $z = |a|$ d) None of the above
- 59 If α, β, γ are the roots of equations $x^3 + Px^2 + Qx + R = 0$,
 Then the value of $\tan^{-1} \alpha + \tan^{-1} \beta + \tan^{-1} \gamma$ is
 a) $n\pi/2$ b) $n\pi$ c) $2n\pi$ d) $\frac{n\pi}{4}$

- 67 The impedance of an inductive reactance varies
- Linearly with frequency
 - Parabolically with frequency
 - Exponentially with frequency
 - Linearly with frequency in an increasing manner
- 68 Two resistance R_1 and R_2 give combined resistance of 4.5 ohms when in series and 1 ohm when in parallel. The resistances are
- 3 ohms and 6 ohms
 - 3 ohms and 9 ohms
 - 1.5 ohms and 3 ohms
 - 1.5 ohms and 0.5 ohms
- 69 Which of the following bulbs will have the least resistance?
- 220V, 60W
 - 220V, 100W
 - 115V, 60W
 - 115 V, 100W
- 70 A resistance of 5 ohms is further drawn so that its length becomes double. Its resistance will now be
- 5 ohms
 - 7.5 ohms
 - 10 ohms
 - 20 ohms
- 71 The power rating of a 470 ohm resistor carrying a current of 40mA should be
- $\frac{1}{4}$ W
 - $\frac{1}{2}$ W
 - 2 W
 - 1W
- 72 Equivalent Resistance between X and Y is



- 75 Ω
- 50 Ω
- 275 Ω
- None of above

- 73 The open-circuit emf of a storage cell is 2.2 volts. The terminal voltage measured when the current is 12A is found to be 1.98 volts. The internal resistance of the cell is
- 0.00183 ohm
 - 0.0183 ohm
 - 0.183 ohm
 - 1.83 ohm
- 74 A capacitor passes a current of 12.6 mA when supplied with 20 V ac with a frequency of 1kHz. The capacitance of the capacitor is
- 0.1 μ F
 - 0.1pF
 - 1 μ F
 - 1F
- 75 The system response can be tested better with
- Sinusoidal input signal
 - Unit impulse input signal
 - Ramp input signal
 - Exponentially decaying signal
- 76 In an ideal op-amp the output impedance is
- 50 ohm
 - 100 ohm
 - Infinite
 - Zero

- 77 What will be dB gain for an increase of power level from 13 to 26W
a) 1 b) 2 c) 8 d) 3
- 78 The oscillator with the best frequency stability and accuracy is
a) Hartley oscillator b) Colpitts Oscillator
c) Tickler feedback oscillator d) Crystal controlled oscillator
- 79 The desirable properties of transformer core material are
a) Low permeability and low hysteresis loss
b) High permeability and high hysteresis loss
c) High permeability and low hysteresis loss
d) Low permeability and high hysteresis loss
- 80 The quality factor of series R-L-C circuit will increase if
a) R decreases. b) R increases.
c) Voltage increases. d) Voltage decreases.