Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

B.E. Sem-III Examination December 2009

Subject code: 130701 Subject Name: Digital Logic Design

Date: 21 /12 /2009 Time: 11.00 am – 1.30 pm

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Convert the following numbers to decimal (i) $(10001.101)_2$ (ii) $(101011.11101)_2$ (iii) $(0.365)_8$ (iv) A3E5 (v) CDA4 (vi) $(11101.001)_2$ (vii) B2D4	**07**
	(b)	Perform the operation of subtractions with the following binary numbers using 2′ complement (i) 10010 - 10011 (ii) 100 -110000 (iii) 11010 -10000	**07**
Q.2	**(a)**	Obtain the simplified expressions in sum of products for the following Boolean functions: (i) $F(A,B,C,D,E) = \sum(0,1,4,5,16,17,21,25,29)$ (ii) A′B′CE′ + A′B′C′D′ +B′D′E′ + B′C D′	**07**
	(b)	Demonstrate by means of truth tables the validity of the following Theorems of Boolean algebra (i) De Morgan's theorems for three variables (ii) The Distributive law of + over-	**07**
		OR	
	(b)	Implement the following Boolean functions (i) F= A (B +CD) +BC′ with NOR gates (ii) F= (A + B′) (CD + E) with NAND gates	**07**
Q.3	**(a)**	Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number.	**07**
	(b)	Discuss 4-bit magnitude comparator in detail	**07**
		OR	
Q.3	**(a)**	With necessary sketch explain full adder in detail	**07**
	(b)	Design a combinational circuit that generates the 9′ complement of a BCD digit,	**07**
Q.4	**(a)**	Discuss D-type edge- triggered flip-flop in detail	**07**
	(b)	Design a counter with the following binary sequence:0,4,2,1,6and repeat (Use JK flip-flop)	**07**
		OR	
Q.4	**(a)**	Design a counter with the following binary sequence:0,1,3,7,6,4,and repeat.(Use T flip-flop)	**07**
	(b)	(i)With neat sketch explain the operation of clocked RS flip (ii)Show the logic diagram of clocked D	**05** **02**
Q.5	**(a)**	With necessary sketch explain Bidirectional Shift Register with parallel load.	**07**
	(b)	Draw the state diagram of BCD ripple counter, develop it's logic diagram, and explain it's operation.	**07**
		OR	
Q.5	**(a)**	Construct a Johnson counter with Ten timing signals.	**07**
	(b)	Discuss Interregister Transfer in detail	**07**

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