Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

B.E. Sem-III Remedial Examination March 2010

Subject code: 130701 **Subject Name: Digital Logic Design**

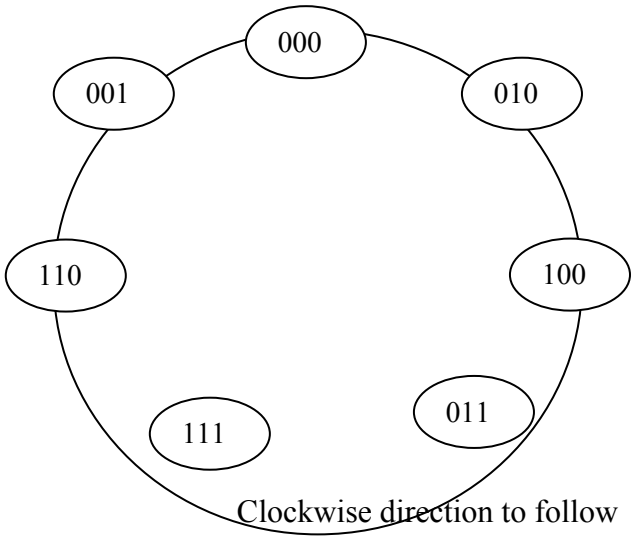
Date:10 / 03 /2010 **Time: 03.00 pm – 0.5.30 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define: Digital System. Convert following Hexadecimal Number to Decimal : B28, FFF, F28 Convert following Octal Number to Hexadecimal and Binary: 414, 574, 725.25	**07**
	(b)	Define : Integrated Circuit and briefly explain SSI, MSI, LSI and VLSI	**07**
Q.2	**(a)**	Draw the logic symbol and construct the truth table for each of the following gates. [1] Two input NAND gate [2] Three input OR gate [3] Three input EX-NOR gate [4] NOT gate	**07**
	(b)	Give classification of Logic Families and compare CMOS and TTL families	**07**
		OR	
	(b)	Explain SOP and POS expression using suitable examples	**07**
Q.3	**(a)**	Design a 4 bit binary to BCD code converter	**07**
	(b)	Design a full adder circuit using decoder and multiplexer	**07**
		OR	
Q.3	**(a)**	Write short note on EEPROM, EPROM and PROM	**07**
	(b)	Define: [1] Comparator [2] Encoder [3] Decoder [4] Multiplexer [5] De-multiplexer [6] Flip Flop [7] PLA	**07**
Q.4	**(a)**	Draw and explain the working of following flip-flops [1] Clocked RS [2] JK	**07**
	(b)	Convert SR flip-flop into JK flip-flop	**07**
		OR	
Q.4	**(a)**	Design sequential counter as shown in the state diagram using JK flip-flops	**07**



	(b)	State and explain the features of register transfer logic	**07**
Q.5	**(a)**	Explain the working of 4 bit asynchronous counter	**07**
	(b)	Explain memory unit	**07**
		OR	
Q.5	**(a)**	Explain the design of Arithmetic Logic Unit	**07**
	(b)	Explain Control Logic Design	**07**

****