



W'05 : 6 FN : EC 406 (1481)

ELECTRONIC CIRCUITS

Time : Three hours

Maximum marks : 100

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

*All parts of a question (a, b, etc) should be
answered at one place.*

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Group A

1. (a) Discuss the need for biasing a transistor. 4

- (b) Define stability factor with reference to BJT amplifier. Draw the circuit diagram of self bias circuit and derive an expression for stability factor. Design a self bias circuit for a silicon transistor having $\beta = 50$. Assume $V_{CC} = 10\text{ V}$, $V_{CE} = 5\text{ V}$, $I_C = 1\text{ mA}$, $R_C = 3.3\text{ k}\Omega$ and $S = 10$. 6 + 4

- (c) Draw the hybrid π model for CE configuration at high frequencies. Explain the significance of each parameter used in the circuit. 6
2. (a) Draw the input and output characteristics of a transistor in CB configuration and explain them. 8
- (b) Discuss the effect of cascading multiple stages of amplifier sections over gain and bandwidth of the overall amplifier. Derive the expressions for overall gain for n -stage cascade system. 6
- (c) Draw the common drain FET amplifier and its equivalent circuit. Determine its voltage gain. 6
3. (a) Draw the circuit diagram of voltage series feedback amplifier and derive the expressions for input and output impedance. 7
- (b) Explain the effect of negative feedback on bootstrapped CE amplifier. 6
- (c) Describe the working of Weinbridge oscillator. Derive the expression for oscillating frequency. 7
4. (a) Draw the transfer characteristics of the basic differential amplifier. Explain its advantages and limitations. 6
- (b) Draw the circuit diagram of a class A transformer coupled power amplifier and explain its operation. Derive an expression for its maximum efficiency. 7
- (c) Explain the origin and magnitude of harmonic distortion in power amplifiers. Explain how even harmonics are eliminated in push-pull amplifiers. 7

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(2)

(Continued)

Group B

5. (a) Find the minimal SOP expression for the function
 $f(A, B, C, D) = \sum m(1, 2, 3, 5, 13) + \sum d(6, 7, 8, 9, 11, 15)$
 Implement the minimized function using NAND gates. 7
- (b) Obtain the simplified product of sums expression using K-map for the function
 $F(A, B, C, D) = \pi(0, 1, 2, 3, 4, 10, 11)$. 4
- (c) (i) Realize EXOR gate using only NOR gates. 3
- (ii) Find the SOP expression for
 $y = AB + \overline{AC} + BC$ 3
- (iii) State and prove de Morgan's theorems. 3
6. (a) Design a decimal to BCD converter and draw its logic diagram. 8
- (b) Implement a full adder circuit with half adders and a OR gate. 4
- (c) Design a BCD to seven segment decoder and implement it using logic gates. 8
7. (a) Draw the circuit diagram of a TTL NAND gate and explain its operation. Distinguish between totem pole output and open collector output. Compare TTL, ECL, MOS, CMOS logic families. 6 + 4
- (b) Draw the circuit of an SR flip-flop using NAND gates and explain its operation. 5

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(3)

(Turn Over)

- (c) Explain the operation of astable multivibrator. 5
8. (a) Design a 4-bit binary up/down ripple counter. 6
- (b) With a neat diagram, explain the operation of a bidirectional shift register. 6
- (c) Draw the diagram and explain the operation of successive approximation type of A/D convertor. 8

Group C

9. Choose the correct answer: 2×10
- (i) The main function of transformer used in the output of a power amplifier is
- (a) To step up the voltage
- (b) To increase the voltage gain
- (c) To match the load impedance with dynamic output resistance of the transistor
- (d) To safeguard the transistor against over-heating
- (ii) An RC phase shift oscillator will not produce any oscillation until and unless the voltage gain of its internal amplifier is
- (a) unity
- (b) less than unity
- (c) around 3
- (d) more than 29

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(4)

(Continued)

- (iii) An op-amp is
- (a) a differential amplifier
- (b) a high gain push-pull amplifier
- (c) a direct coupled amplifier
- (d) a low impedance amplifier
- (iv) In an amplifier if conducts during the cycle from 0° to 90° and again from 180° to 270° , the amplifier will be termed as
- (a) class A
- (b) class B
- (c) class C
- (d) class AB
- (v) Which of the following is ideally suited for choppers ?
- (a) JFET
- (b) BJT
- (c) UJT
- (d) SCR
- (vi) The NAND-NAND realization is equivalent to
- (a) AND-NOT realization
- (b) AND-OR realization

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(5)

(Turn Over)

- (c) OR-AND realization
- (d) NOT-OR realization
- (vii) The logic family which has minimum power dissipation is
- (a) TTL
- (b) PL
- (c) ECL
- (d) CMOS
- (viii) The minimum number of bits required to represent negative numbers in the range of - 1 to - 9 using two's complement representation is
- (a) 2
- (b) 3
- (c) 4
- (d) 5
- (ix) A combinational circuit
- (a) always contains memory elements
- (b) never contains memory elements
- (c) may sometimes contain memory elements
- (d) contains only memory elements
- (x) A ring counter consisting of five flip-flops will have
- (a) 5 states
- (b) 10 states
- (c) 32 states
- (d) infinite states

S'06 : 6 FN : EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum marks : 100*

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Group A

1. (a) What is the need for biasing a transistor? What do you mean by operating point? 2
- (b) Draw the circuit of self-bias circuit and explain how it fixes the operating point? 8
- (c) Draw the circuit of common source FET amplifier and using the a.c. equivalent circuit obtain the expression for its voltage gain. 10
2. (a) With the help of suitable circuit, explain the effect of coupling and device capacitors on the frequency response of R-C coupled BJT (bipolar junction transistor) amplifier. 10
- (b) An amplifier with open-loop voltage gain $A_v = 1000 \pm 100$ is available. It is necessary to have an amplifier whose voltage gain varies by no more than ± 0.1 per cent. Design the circuit.

- (i) Find the reverse transmission factor β of the feedback network used in the above problem.
- (ii) Find the voltage gain with feedback of the circuit designed as above. 10
3. (a) Draw and explain the circuit of Wein bridge oscillator and derive an expression for its frequency of oscillation. 10
- (b) Draw a circuit of voltage series feedback amplifier and derive the expression for its input impedance. 10
4. (a) Draw the circuit of differential amplifier with constant current biasing arrangement. Also, draw its transfer characteristics and explain. 10
- (b) Explain the operation of the full-wave rectifier circuit with capacitor filter with the help of relevant waveforms. 7
- (c) Discuss about distortion in amplifiers. 3

Group B

5. (a) Prove that $\overline{AB + BC + CA} = (\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A})$. 4
- (b) Prove that NAND is a universal gate. 3
- (c) Draw the EX-OR gate (two input) realization using only two input NOR gates. 3
- (d) Draw the TTL NAND gate circuit and explain its operation. 10
6. (a) Simplify the following function using K-map and draw the logic gate realization of the corresponding circuit.
 $f(a, b, c, d) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$. 7

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(2)

(Continued)

- (b) Express the decimal number 416 in (i) excess three code, (ii) BCD code, and (iii) binary code. 1+1+1
- (c) Draw the circuit of 3 bit ripple counter and explain its operation using timing diagram. 6
- (d) Draw the circuit of 3 bit weighted resistor type DAC and obtain the expression for its output voltage in terms of its input. 4
7. (a) Write the truth table of full adder and obtain the expression for Sum and Carry. 5
- (b) Draw the circuit of a sequential circuit and explain its operation. 10
- (c) Obtain the excitation table for JK flip-flop from its truth table. What do you mean by race around problem? 5
8. (a) Explain the function of successive approximation type ADC circuit with the help of diagram. 6
- (b) Design a synchronous counter using J-K flip-flop to count in the random sequence 0, 1, 3, 2, 5, 6, 0, 1, 3, 8
- (c) Draw the circuit of astable multivibrator circuit and explain its operation. 6

Group C

9. Choose the *correct* answer or answer as directed: 2×10
- (i) In the hybrid-II model for the transistor in CE configuration r_{bb} is used to account for the
- (a) increased recombination base current
- (b) broad frequency reaction
- (c) bias resistance
- (d) ohmic base-spreading resistance

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(3)

(Turn Over)

- (ii) The BJT amplifier which offers highest input impedance and least voltage gain is
- (a) CE
 - (b) CB
 - (c) CC
 - (d) cascade amplifier
- (iii) Why are R-C oscillators not used at R.F. frequencies?
- (iv) Cascading of amplifiers results in
- (a) increased gain and increased bandwidth
 - (b) increased gain and reduction in bandwidth
 - (c) increased input impedance decreased output impedance
 - (d) decreased input impedance and increased gain
- (v) Why is resonant circuit (parallel) used as load in class-C power amplifiers?
- (vi) Minimum number of two input NAND gates required to realize the logic function $(A\bar{B} + \bar{A}B)$ is
- (a) 5
 - (b) 3
 - (c) 6
 - (d) 4
- (vii) The capacity of a memory chip is 8192 bits. It has 2048 rows. Then the organization of the chip is
- (a) word organized
 - (b) byte organized
 - (c) nibble organized
 - (d) bit organized

- (viii) The multivibrator circuit which possesses one stable state and one quasi-stable state is
- (a) astable
 - (b) monostable
 - (c) bi-stable
 - (d) Schmitt trigger circuit
- (ix) The logic circuit which belongs to non-saturated logic is
- (a) ECL
 - (b) TTL
 - (c) CMOS
 - (d) NMOS
- (x) The ILSB value of a 8 bit DAC whose full scale value is 9.96 V is
- (a) 0.389 V
 - (b) 0.389 mV
 - (c) 0.0389 microvolts
 - (d) 0.0389 V.

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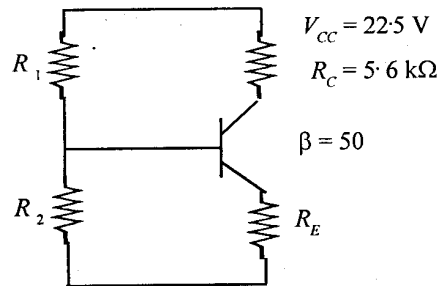
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Group A

1. (a) Briefly explain the reason for keeping the operating point of a transistor fixed. 4
- (b) Draw the voltage divider bias circuit and derive an expression for stability factor. 8
- (c) A transistor with $\beta = 50$, $V_{BE} = 0.7 \text{ V}$, $V_{CC} = 22.5 \text{ V}$, $R_C = 5.6 \text{ k}\Omega$ is used in a biasing circuit as given below :



It is designed to establish the operating point at (V_{CC}, I_C) at $(12\text{ V}, 1.5\text{ mA})$, and stability factor $S \leq 3$. Find the values of the biasing resistor R_1 and R_2 and the emitter resistor R_E . 8

2. (a) What are the characteristics and uses of a common base transistor amplifier? 4

(b) With a neat circuit diagram, explain the working of a transistor amplifier in which phase inversion of the input signal does not take place. Obtain the expression for input resistance of this amplifier. 8

(c) What are the advantages of a transformer coupled amplifier? Find the overall voltage gain of a two-stage transformer-coupled amplifier in terms of the turns ratio of the coupling transformer. 8

3. (a) What is the difference between a voltage amplifier and a power amplifier? 4

(b) Derive the conversion efficiency of a class B power amplifier and clearly explain the reason. Why are most of the power amplifiers used in practice designed to operate in class AB stage? 8

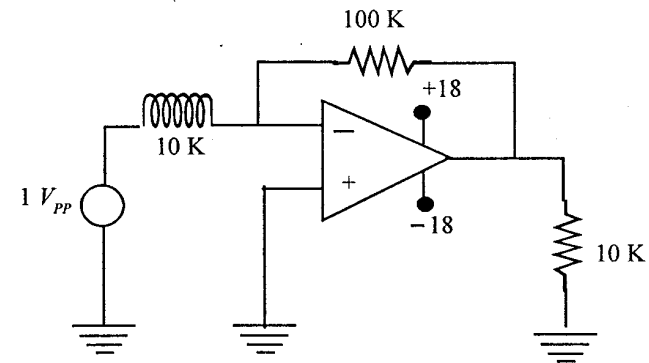
(c) A transistor rated for a maximum collector dissipation of 100 W operates a single ended class A output stage from a 10 V supply. Calculate the approximate values of (i) maximum undistorted ac power output, (ii) the quiescent current, and (iii) turns ratio of the output transformer.

Assume load resistance of $16\ \Omega$ and overall collector efficiency as 0.5. 8

4. (a) Explain, with neat circuit diagram, the working of a phase shift oscillator using three sections of RC network. State the expression for the frequency of oscillations and minimum gain of the amplifier for sustained oscillations. 8

(b) Draw the circuit of a summing operational amplifier using inverting amplifier configuration. Write an equation for the output voltage for this circuit. 6

(c) For the circuit shown below, find the closed loop gain, input impedance, common mode rejection ratio, and maximum operating frequency.



Given: $A_{cm} = 0.001$, $A_{OL} = 180,000$, $Z_{in} = 1\text{ m}$, $Z_o = 80\ \Omega$, slew rate = $0.5\text{ V}/\mu\text{s}$. 6

Group B

5. (a) Write the equivalent of the following expressions: 2

(i) $(00011011)_2 = (?)_{10}$

(ii) $(356)_8 + (275)_8 = (?)_8$

(b) Realise the following expression using logic gates: 4

$Y = \overline{A + B} + \overline{C}$

$Y = \overline{AC} \cdot \overline{BC}$

(c) Simplify the following Boolean expression: 6

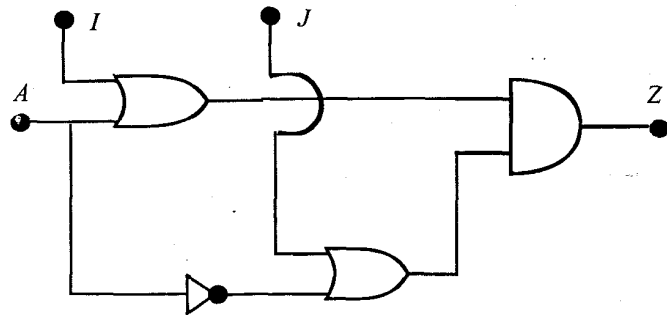
$$T(x, y, z) = (x + y) [\bar{x}(\bar{y} + \bar{z})] + \bar{x}\bar{y} + \bar{x}\bar{z}$$

(d) Why is deMorgan's theorem important in the simplification of Boolean expressions? Use deMorgan's theorem to prove that a NOR gate with inverted inputs is equivalent to an AND gate. 8

6. (a) Simplify the following Boolean expression using minimum number of 3-input NAND gates: 5

$$f(A, B, C, D) = \Sigma(1, 2, 3, 4, 7, 9, 10, 12)$$

(b) The circuit shown below is used to implement the function $z = f(A, B) = A + B$. What should be the values of I and J ? 5



(c) Explain the NAND gate and NOR gate latches with truth table and logic symbol. 10

7. (a) Explain parallel data transfer and serial data transfer for 3 bits. 8

(b) Explain the operation of a half adder circuit with the aid of truth table. Realise a full adder using half adders and OR gates. 6

(c) Construct a binary counter that will convert a 64 kHz signal into a 2 kHz square wave. 6

8. (a) Discuss in detail the IC logic families—TTL, ECL and CMOS, with respect to circuit, speed, noise immunity and power dissipation. 8

(b) Compare the Weighted Resistor Method and R-2R Ladder for Digital to Analog conversion. Derive the output equation. 8

(c) What are Programmable Logic Arrays. 4

Group C

9. Choose the correct answer for the following: 10 × 2

(i) The voltage divider biasing circuit is used in amplifiers quite after because it

- (a) limits the ac signal going to the base.
- (b) makes the operating point almost independent of β .
- (c) reduces the dc base current.
- (d) reduces the cost of the circuit.

(ii) Which of the following statement is not correct regarding h parameters of a transistor?

- (a) Values of h parameters can be obtained from transistor characteristics.
- (b) Values depend on transistor configuration.
- (c) Values depend on operating point.
- (d) They are four in number.

- (iii) The major advantage of d.c. amplifiers is that it
- (a) uses less number of components.
 - (b) has very good temperature stability.
 - (c) does not use frequency sensitive components.
 - (d) can amplify direct current and low frequency signals.
- (iv) Crystal oscillators are superior to tuned LC oscillators mainly because of their
- (a) high degree of frequency stability.
 - (b) size of the crystal.
 - (c) availability of crystal.
 - (d) high Q value.
- (v) The voltage gain of an ideal voltage follower is
- (a) 1
 - (b) < 1
 - (c) 0
 - (d) ∞
- (vi) The number of bits required to represent an eight digit decimal number in BCD is
- (a) 8
 - (b) 16
 - (c) 24
 - (d) 32
- (vii) The output of a AND gate is high if
- (a) both inputs is low.
 - (b) one input is high and the other is low.
 - (c) both inputs are high.
 - (d) none of the above.
- (viii) Which of the following flip-flops is used as a latch ?
- (a) JK flip-flop
 - (b) RS flip-flop
 - (c) D flip-flop
 - (d) T flip-flop
- (ix) A full adder can be made of
- (a) two half adders.
 - (b) two half adders and a NOR gate.
 - (c) two half adders and a OR gate.
 - (d) two half adders and a AND gate.
- (x) To serially shift a byte of data into a shift register, there must be
- (a) one clock pulse.
 - (b) one load pulse.
 - (c) eight clock pulses.
 - (d) one clock pulse for each one in the data.

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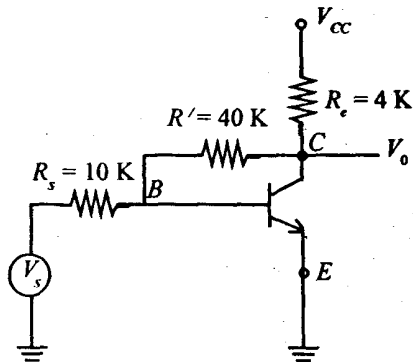
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Group A

1. (a) Neatly draw the fixed-bias circuit for an NPN transistor and explain its operation. 6
- (b) What are the principal causes of instability of a fixed bias circuit? Discuss with suitable explanation. 6
- (c) For a self biased NPN transistor with $\beta = 55$ and $V_{BE} = 0.65$, $R_1 = 90\text{ K}$, $R_2 = 10\text{ K}$, $R_c = 5.6\text{ K}$, $R_e = 1\text{ K}$. If the supply voltage = 22.5 V find the Q-point. 8

2. (a) Define the four h -parameters for the small signal model of a bit at low frequency and give the analytical expression for each. 8
- (b) Derive the current gain (A_I), amplification of voltage (A_v), input impedance (Z_i) and output admittance (Y_o) in terms of the h -parameters and load resistance Z_L . If the source resistance R_s is taken into account how will the voltage amplification factor change? 12
3. (a) Analyse the circuit given below using the concept of feedback, provided that $h_{ie} = 1.1 \text{ K}$, $h_{fe} = 50$, $h_{re} = h_{oc} = 0$ to find out A_{vf} and R_{if} . 12



- (b) Derive how the input and output resistance are changed in (i) voltage series feedback, and (ii) current shunt feedback. 8
4. (a) Design a non-inverting summing amplifier using a single op-amp and explain its operation. 8

- (b) Distinguish between class A, class B, class AB and class C operation of an amplifier with suitable figures. 8
- (c) Show that the maximum efficiency of class A amplifier cannot be more than 25%. 4

Group B

5. (a) Simplify the following Boolean expression to sum of minterm form using suitable theorem: 5 × 2
- (i) $(A + B + C + D)(A + B + C + E)(A + B + C + F)$
- (ii) $\overline{(A + B + C)(A + \bar{B} + \bar{C})}$
- (b) Convert the following numbers: 5 × 2
- (i) $(0.513)_{10}$ to octal
- (ii) $(0.6875)_{10}$ to binary
6. (a) Simplify the following using K map 5 × 2
- (i) $\Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$
- (ii) $\bar{A}\bar{B}\bar{C} + \bar{B}\bar{C}\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}$
- (b) Design a 4-bit carry look ahead generator and using it design a 4-bit carry look ahead adder. Give suitable figures and explain the operation. 10
7. (a) Design a 4-bit modulo sixteen synchronous counter using $4 \times$ T-flip-flops and parallel carry. Explain its operation. 10

- (b) Explain the operation of a 3-input TTL NAND gate that uses a multiemitter transistor and totem-pole structure which supports active pull-up. 10
8. (a) Define (i) resolution, (ii) accuracy, (iii) linearity of an A/D converter. 6
- (b) Explain the operation of an R-2R type D/A converter with suitable circuit diagram. 10
- (c) What are the advantages of an SAR type A/D converter and what are the disadvantages of it over a parallel or flash type A/D converter. 4

Group C

9. Write the *correct* answer for the following: 2 × 10
- (i) The symbol α in terms of bjt denotes
- (a) ratio of I_B and I_C
- (b) ratio of V_{BE} and V_{CE}
- (c) ratio of I_E and I_C
- (d) ratio of I_C and I_E
- (ii) In the context of BJT, α and β are related by
- (a) $\beta = 1 + \alpha$
- (b) $\alpha = \beta / \beta + 1$
- (c) $\beta = \alpha / 1 + \alpha$
- (d) None of the above

- (iii) Negative feedback is used to
- (a) increase the gain
- (b) increase stability
- (c) design an oscillator
- (d) All of the above
- (iv) Ideal voltage op-amp has
- (a) infinite o/p resistance and gain
- (b) infinite i/p resistance and gain
- (c) negligible o/p resistance and CMRR
- (d) All of the above
- (v) The following configuration has maximum conversion efficiency
- (a) class-A amplifier
- (b) class-AB amplifier
- (c) class-B amplifier
- (d) class-C amplifier
- (vi) The fastest saturating logic is
- (a) ECL
- (b) CMOS

- (c) I^2L
- (d) TTL
- (vii) The both 1 state is forbidden for
- (a) JK flip-flop
- (b) D flip-flop
- (c) RS flip-flop
- (d) T flip-flop
- (viii) The fastest A/D converter is
- (a) Flash type
- (b) SAR type
- (c) Dual slope type
- (d) None of the above
- (ix) The following operation is associative
- (a) NAND
- (b) NOR
- (c) Both NAND and NOR
- (d) EX-OR
- (x) Stability can be improved in an op-amp by
- (a) pole zero compensation
- (b) dominant pole compensation
- (c) lead compensation
- (d) All of the above

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Group A

1. (a) For a single-stage transistor amplifier operated at low frequency,

$$h_{ie} = 1100 \Omega, \quad h_{re} = 2.5 \times 10^{-4}, \quad h_{fe} = 50, \\ h_{oe} = 24 \mu\text{A/V}.$$

(i) What is the maximum value of R_L for which R_i differs by not more than 10% of its value at $R_L = 0$? 5

(ii) What is the maximum value of R_s for which R_o differs by not more than 10% of its value at $R_s = 0$? 5

- (b) For the circuit shown in Fig. 1, find the voltage gain V_o/V_s as a function of R_s , b , R_e and R_L .

Assume that $h_{oc} = (R_c + R_L) \leq 0.1$. 10

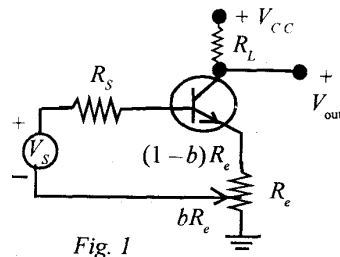


Fig. 1

2. (a) For the two sets of input to a differential amplifier
 Set 1: $v_1 = +50 \mu\text{V}$, $v_2 = -50 \mu\text{V}$
 Set 2: $v_1 = 1050 \mu\text{V}$, $v_2 = 950 \mu\text{V}$
 if the CMPR is 1000, calculate the percentage difference in output voltage (with respect to set 1) of input signals. 6

- (b) In a push-pull amplifier system, the input (base current) to transistor Q_1 is $x_1 = X_m \cos \omega t$ and the input to the transistor Q_2 is $x_2 = -X_m \cos \omega t$. The collector current in each transistor may be expressed as

$$i_c = I_c + a_1 x + a_2 x^2 + a_3 x^3 + \dots$$

Find the output current of push-pull amplifier and comment. 6

- (c) An inverting amplifier is shown in Fig. 2:

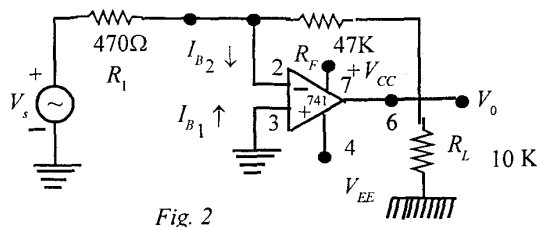


Fig. 2

Determine the possible output offset voltage due to input offset voltage V_{io} and input bias current I_B . Also, find the value of R on needed to reduce the effect of input bias current. 8

3. (a) Explain the condition to prevent thermal runaway. Also, find the value of thermal resistance, θ , required for Ge transistors in self-bias circuit as shown in Fig. 3 in order that circuit is stable.

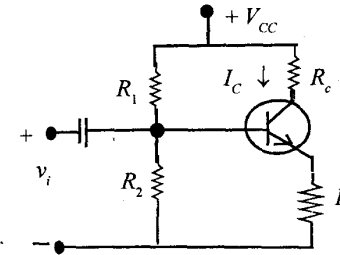


Fig. 3.

Assume $V_{cc} = 30 \text{ V}$, $R_c = 2 \text{ K}$, $R_e = 4.7 \text{ K}$. Also, assume I_c increases by 0.131 mA over a temperature range of 25°C to 75°C . 12

- (b) Explain the electrical model of a piezoelectrical crystal. Assume that the crystal has following parameters:
 $L = 0.33 \text{ H}$, $C = 0.065 \text{ pF}$, $c' = 1 \text{ pF}$, $R = 5.5 \text{ K}$ in series arm and shunt arm, respectively.
 (i) Find the series resonant frequency; and
 (ii) By what percent does the parallel resonant frequency exceed the series resonant frequency? 8

4. (a) For a voltage amplifier without feedback, discuss the condition on its input and output resistance for stability. Also, show that, after incorporating negative feedback, into it, it becomes more stable. 10

(b) A circuit is shown in Fig. 4:

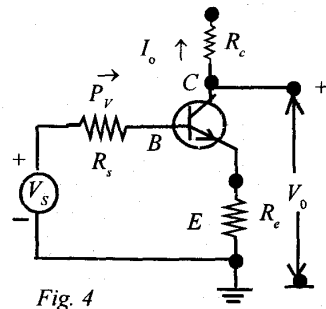


Fig. 4

Verify that it is current series feedback amplifier. 10

Group B

- (a) (i) Represent $(-17)_{10}$ in sign magnitude, one's complement and two's complement representation.
- (ii) Convert the given binary number in octal number: 11001110001.000101111001
- (iii) Obtain decimal equivalent of hexadecimal number $(3A.2F)_{16}$
- (iv) Subtract $(5C)_{16}$ from $(3F)_{16}$. 1 x 4
- (b) Design a binary-to-grey code converter for first 16 numbers by using minimum number of gates. 6
- (c) Design a full-adder circuit using two half adders as (i) block diagram of HA only; and (ii) circuit diagram of HA. Then in the second case, determine the propagation delay time for sum output (S_n) and carry output (C_n), assuming propagation delay of gates as: EX-OR gates = 20 ns; AND gates = 40 ns. and OR gates = 10 ns. 3+3+4

6. (a) A circuit is shown in Fig. 5 ($V_m = 1 V_{pp}$ sine wave):

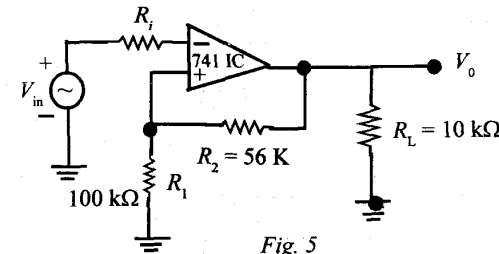


Fig. 5

OP AMP is 741 type with supply voltage $\pm 15V$. Determine the threshold voltages V_{UT} and V_{LT} , i.e., upper and lower threshold voltages, and hysteresis voltage $V_{HY} = 50 mV$. Also, draw the output waveform. Given for IC 741, the maximum output voltage swing is $\pm 14 V$. 10

(b) The NOR gate feeds 5 gates as shown in Fig. 6

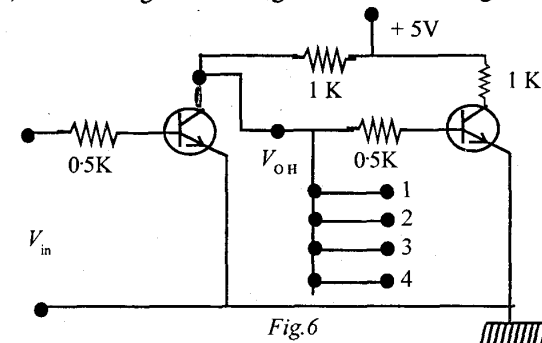


Fig.6

What should be the minimum value of β to drive all the gates to saturation. Given: 10

$$V_{BE}(\text{sat}) = 0.8 V$$

$$V_{CE}(\text{sat}) = 0.2 V.$$

7. (a) Design a synchronous binary up-down decade counter using JK flip-flops. 10

(b) Figure 7 shows the clock waveform and input waveform applied to *D* or *J* input to each of the following type of flip-flops:

- (i) Positive edge triggered *D*-type FF (7474)
- (ii) Positive level triggered *D*-type FF (7475)
- (iii) Negative edge triggered JKFF (74112).

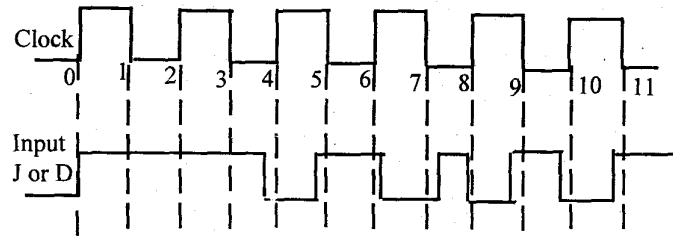


Fig. 7

Sketch the outputs of the respective flip-flops. 10

8. (a) Explain dual slope A/D converter with a proper block diagram. Compare its relative merits and demerits with respect to that of successive approximate type. 10

(b) Consider a 4-bit unipolar D/A converter with $V(1) = -1\text{ V}$ and $V(0) = 0\text{ V}$ and $R_F = 8R$ (Fig. 8):

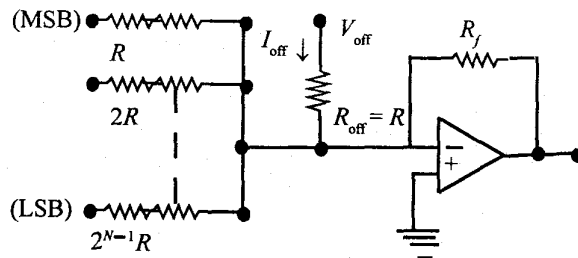


Fig. 8

(i) Obtain the analog output voltage for each of the digital input from 0000 to 1111.

(ii) Adjust the offset voltage, as shown in Fig. 8, such that $V_0 = 0\text{ V}$ for a digital input of 1000. With this offset, obtain the analog output voltage for each of the digital inputs. 10

Group C

9. Choose the correct answer for the following: 2 × 10

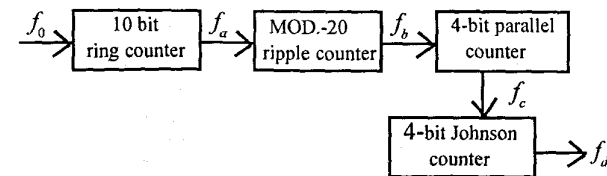
(i) In a 4 stage ripple counter, propagation delay of FF is 50 ns. If the pulse width of strobe is 30 ns, find the maximum frequency at which the counter operates reliably.

- (a) 12.5 MHz
- (b) 50 MHz
- (c) 5.88 MHz
- (d) 4.35 MHz

(ii) The problem of current hogging is associated with

- (a) TTL gates
- (b) ELL gates
- (c) RTL gates
- (d) None of the above

(iii) For the circuit, the frequency f_d is



- (a) 16 Hz
 (b) 4 Hz
 (c) 2 Hz
 (d) None of the above
- (iv) Total number of Boolean functions that can be generated with $n = 4$ variable is
- (a) 14437
 (b) 65536
 (c) 16342
 (d) 25651
- (v) The input to a 4-channel MUX have the following characteristics
 channel 1 : 50 Hz
 channel 2 : 200 Hz
 channel 3 : 75 Hz
 channel 4 : 90 Hz
 The minimum sampling rate of MUX is
- (a) 1600 Hz
 (b) 200 Hz
 (c) 400 Hz
 (d) None of the above
- (vi) In CMOS inverter made up of two transistors,
- (a) both transistors are n -channel and are enhanced type.
 (b) one transistor is n -channel and other is p -channel. Both are of depletion type.
 (c) both transistors are p -channel and are of depletion type.
 (d) None of the above.
- (vii) For a number of transistor switches, which are direct-coupled,
- (a) both rise time and full time increases.
 (b) rise time increases and full time decreases.
 (c) rise time decreases and full time increases.
 (d) None of the above.
- (viii) In regard to FET,
- (a) in p -channel depletion mode in the active region, the control voltage is negative.
 (b) in n -channel depletion mode in the active region, the control voltage is negative.
 (c) NMOS in enhancement mode is cutoff for $V_{GS} < 0$.
 (d) None of the above.
- (ix) About feedback amplifier, choose the correct statement :
- (a) If the feedback is termed as regenerative, then gain with feedback should have magnitude greater than gain without feedback.
 (b) Transconductance amplifier with voltage shunt feedback has output quantity as voltage and input quantity as current.
 (c) For current series feedback amplifier, the output resistance with feedback is less than output resistance without feedback.
 (d) None of the above

(x) In connection with oscillators.

- (a) In every oscillator the loop gain is slightly larger than unity.
- (b) Oscillation will sustain, if product of transfer gain of amplifier and magnitude of feedback gain at the oscillator frequency is less than unity.
- (c) In Hartley oscillators, two series capacitors connected in parallel with an inductor.
- (d) None of the above.

ELECTRONIC CIRCUITS*Time : Three hours**Maximum marks : 100*

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

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answered at one place.*

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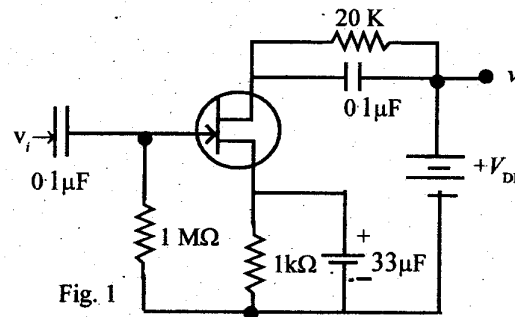
*Any missing or wrong data may be assumed suitably
giving proper justification.*

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Figure 1 shows a JFET being used as a common source a.c. amplifier. Given the following specifications for the JFET used :

$$C_{gs} = 8 \text{ pF}; C_{gd} = 4 \text{ pF}; C_{ds} = 2 \text{ pF}; r_d = 20 \text{ k}\Omega;$$
$$g_{fs} = 1000 \text{ micro-mhos.}$$



Determine the total input capacitance (C_i).

8

- (b) For the given clamping circuit and the input waveform as shown (Fig. 2), draw the output waveform. 6

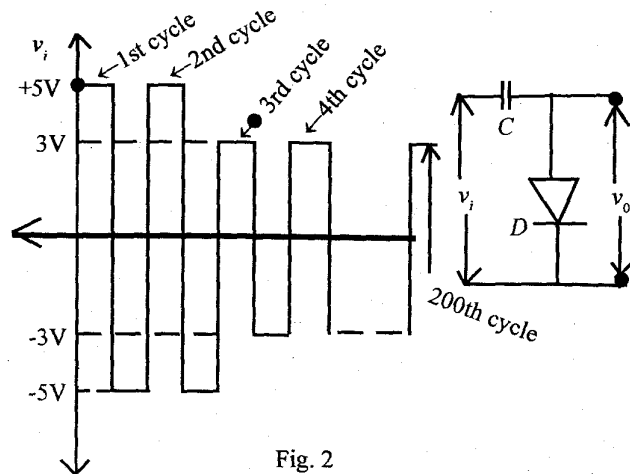


Fig. 2

- (c) A single stage CE amplifier has a lower 3 dB cut-off of 64 Hz and an upper 3 dB cut-off of 10 kHz. What will be the new value for these frequencies for two stage amplifier consisting of a cascaded arrangement of two identical stages of the type mentioned. 6
2. (a) Draw the circuit of an RC phase shift oscillator using an FET. Derive an (i) expression for the frequency of oscillations, and (ii) condition for sustained oscillations. 10
- (b) Draw the electrical equivalent circuit of a quartz crystal explaining the significance of various components of the circuit. Also, draw the neat sketches of impedance frequency, reactance vs. frequency of the quartz resonator indicating the critical frequency and their values. 10

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(2)

(Continued)

3. (a) A class B transformer coupled amplifier is to supply 4 W to a 10Ω load; $V_{cc} = 30 \text{ V}$; the transformer efficiency is 75%. Specify the output transformer and output transistors. 10
- (b) Draw a fixed bias circuit and a self-bias circuit, using a BJT, and mention typical component value and supply voltage for the circuit. Also, explain why bias stabilization is done in a bipolar function transistor amplifier circuit. 10
4. (a) Explain the operation of the circuit shown in Fig. 3: 10

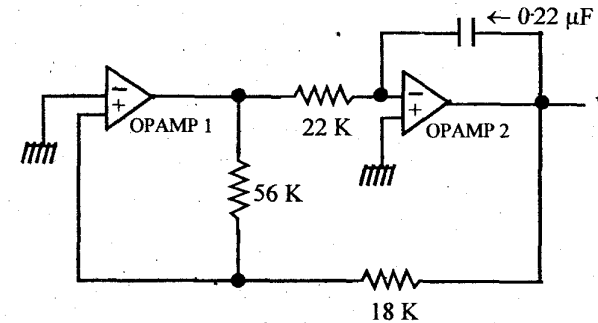


Fig. 3

What type of signal does it produce? Determine the frequency of the output signal. How can one change the frequency of the signal to 10 kHz? 10

- (b) Establish the difference between the following: 10
- (i) CE, CB and CC configurations
- (ii) Voltage-series, voltage-shunt, current series and current shunt feedback
- (iii) Class A, Class B and Class C with the help of suitable examples and diagrams.

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(3)

(Turn Over)

Group B

5. (a) Simplify the following Boolean expressions to sum of product form: 6
- (i) $\bar{X}\bar{Y}\bar{Z} + \bar{X}YZ + X\bar{Y}\bar{Z} + XYZ$
- (ii) $AB + \overline{AC} + \overline{ABC}(AB + C)$
- (iii) $\overline{XY} + \bar{X} + XY$
- (iv) $\overline{ABCD} + \overline{ABCD} + \overline{ABCD} + \overline{ABCD}$
- (b) Draw the logical circuits for the following using NOR gates only: 3 × 2
- (i) $(X + Y) \cdot (\bar{X} + Y) \cdot (\bar{X} + \bar{Y})$
- (ii) $(A + B)(B + C)(\bar{C} + \bar{A})$
- (iii) $(\bar{X} + Y) + (\bar{Y} + Z) + (\bar{Z} + X)$
- (c) Obtain a simplified form of the Boolean expression $F(u, v, w, z) = \Sigma(0, 2, 3, 4, 7, 9, 10, 13, 14, 15)$ using Karnaugh map. Also, draw the logical circuit for the simplified function using NAND gates. 8
6. (a) Design a 3-bit modulo 8 synchronous counter. Also, explain its operation. 8
- (b) Design a binary to grey code converter for first 16 numbers by using minimum number of gates. 6
- (c) Design a full subtractor circuit using half subtractors as (i) block diagram of HS; and (ii) circuit diagram of HS. 6
7. (a) Design a ripple counter using JK flip-flops. Also, list the set of rules for designing a ripple counter using JK flip-flop. 10

- (b) Draw a Schmitt trigger circuit and explain its working. Also, describe its application in digital electronics. 10

8. Establish a comparative study between the following:
- (a) RTL, DTL, TTL, ECL logic families in a tabular form on at least six parameters. 6
- (b) RS and JK, master slave JK flip-flops.
- (c) Astable, monostable and bistable multivibrators. 4

Group C

9. Choose the *correct* answer for the following: 2 × 10
- (i) Four CB stages were cascaded together to get an overall gain of 100. Assuming that cascading is direct, could you give an idea of gain per stage?
- (a) Yes, it will be 100 only.
- (b) It is 25
- (c) It is $(100)^{1/4}$
- (d) It is indeterminate.
- (ii) Conversion efficiency of a single-stage amplifier is given by
- (a) $\frac{\text{a.c. power delivered to load}}{\text{d.c. power delivered to active device}}$
- (b) $\frac{\text{a.c. power at the output}}{\text{a.c. power at the input}}$
- (c) $\frac{\text{output voltage}}{\text{input voltage}}$
- (d) None of the above

(iii) Type of distortion in which different frequency signals are amplified by different amounts is called

- (a) harmonic distortion
- (b) frequency distortion
- (c) intermodulation distortion
- (d) None of the above

(iv) A square wave signal was applied to an amplifier with a very good low frequency response but a very poor high frequency response. The output waveform had

- (a) suffered severe distortion throughout.
- (b) suffered severe distortion along the vertical edges with fairly good flat region.
- (c) suffered severe distortion of flat region with fairly good reproduction of vertical edges
- (d) None of these.

(v) An amplifier's power level is changed from 8 W to 16 W. The equivalent dB gain is

- (a) 2 dB
- (b) 6 dB
- (c) 3 dB
- (d) 5 dB

(vi) h -parameters of a transistor

- (a) are constant.
- (b) vary with temperature.
- (c) are dependent upon collector current.
- (d) None of the above.

(vii) Each of the following Boolean expression can be implemented using a single logic gate except following one of them :

- (a) $z = \overline{(x + y)}$
- (b) $z = \overline{(x \cdot y)}$
- (c) $z = x \cdot \bar{y} + y \cdot \bar{x}$
- (d) $z = x \cdot y + (x + y) + (\bar{x}y + \bar{y}x)$

(viii) A counter does not find a place in one of the following A/D converter types :

- (a) Successive approximation type A/D converter
- (b) Tracking type A/D converter
- (c) Counter type A/D converter
- (d) Flash type A/D converter

(ix) A full subtractor can be constructed from two half subtractors and

- (a) 2-input NAND.
- (b) 2-input NOR.
- (c) 2-input OR
- (d) 2-input AND.

(x) The basic RS flip-flop is

- (a) a monostable multivibrator
- (b) a bistable multivibrator
- (c) an astable multivibrator
- (d) a Schmitt trigger.

ELECTRONIC CIRCUITS*Time : Three hours**Maximum Marks : 100*

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Figures on the right-hand side margin indicate full marks.

Group A

- Identify the type of feedback with reason shown in Fig. 1. Draw the amplifier circuit without feedback but taking loading effect of feedback network. Determine overall voltage gain, input impedance and output impedance by feedback method.

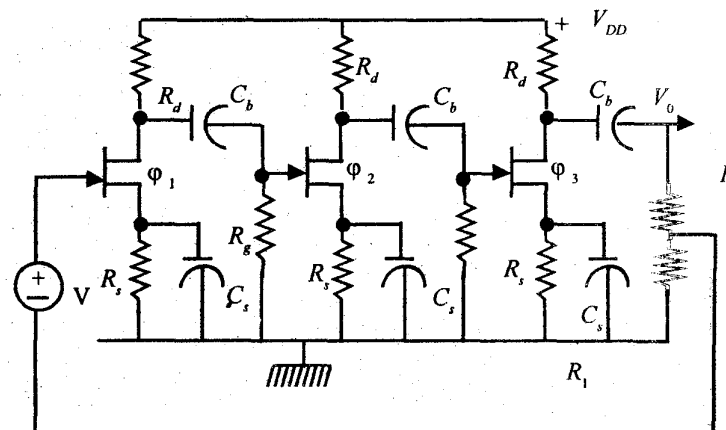


Fig. 1

Given: $R_1 + R_2 = R_g = 1 \text{ M}$, $s_d = 10 \text{ K}$, $R_1 = 40 \Omega$,
 $g_m = 6 \text{ mA/V}$. All FETs are identical with above g_m ,
 s_d , $R_d = 50 \text{ K}$. Neglect capacitive reactances. Derive all the
relations used. Calculate two output impedances R_{of}
and R_{of}' . 20

2. (a) It is desired to have a low 3 dB frequency of not more than 10 Hz for an RC coupled amplifier for which $R_c = 1 \text{ K}$. What is minimum value of coupling capacitance required where transistors with $h_{ie} = 1 \text{ K}$ and $1/h_{oe} = 40 \text{ K}$ are used. Also, $R_1 = R_2 = 20 \text{ K}$. Derive the relation used. 15

(b) Discuss various types of distortions in amplifiers. 5

3. Draw the circuit diagrams of

- (i) Fixed bias common emitter (CE)
(ii) Collector to fixed bias CE amplifier
(iii) Self-biased CE amplifier.

Derive S_I , S_V , S_B for each case. Also, explain physically and mathematically how thermal stability is improved for collector to base biasing and self-biasing. 20

4. Write notes on the following: 4×5

- (i) Push pull class B amplifier
(ii) RC phase shift oscillator
(iii) Analog computer using op amp
(iv) Small signal analysis of FET.

Group B

5. Discuss flash type A/D converter in detail. 20
6. Describe a full adder circuit. Design the circuit with NAND gates only. 20
7. (a) Implement $Y = AB + CD$ from NAND gates only. 6
(b) Minimise by Karnaugh map the following: 5

$$F = \sum (0, 1, 2, 3, 8, 9, 10, 11) + \sum_d (12, 13).$$

- (c) Express $Y = A + BC$ in sum of the product and product of the sum form. 9

8. Write notes on the following: 4×5

- (a) Synchronous counter with J-K master slave flip-flops.
(b) D/A converter with R-2R ladder network
(c) CMOS AND and OR gates.
(d) Astable and monostable multivibrator.

Group C

9. Choose the *correct* answer for the following: 10×2

- (i) Bias stability, SI, of fixed bias circuit is

- (a) 51
(b) 1
(c) 0
(d) infinity

- (ii) Overall voltage gain of emitter follower is
- infinity
 - zero
 - unity
 - None of the above
- (iii) For operational amplifier,
- input impedance infinity and also output impedance.
 - input impedance infinity and zero output impedance.
 - both input and output impedance low.
 - None of the above
- (iv) For ideal difference amplifier,
- CMRR is zero.
 - CMRR is 1.
 - CMRR is -1.
 - CMRR is infinite.
- (v) Ripple factor of fullwave rectifier is
- 0
 - 1.21
 - 0.48
 - None of the above
- (vi) Modulo 6 asynchronous counter uses
- four flip-flops
 - eight flip-flops
 - three flip-flops
 - two flip-flops
- (vii) A counter does not find a place in *any one* of the following A/D converter :
- Successive approximation
 - Flush type
 - Counter type
 - Tracking type
- (viii) The basis R-S flip-flop is
- a monostable multi
 - a bistable multi
 - an astable multi
 - a Schmitt trigger
- (ix) Which one of the following is correct ?
- $h_{fe} = \alpha$
 - $h_{fe} = \beta$
 - $h_{fe} = -\beta$
 - $h_{fe} = -\alpha$

$$(a) \overline{ABC} = \overline{A}\overline{B}\overline{C}$$

$$(b) \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$$

$$(c) \overline{A+B} = \overline{A} + \overline{B}$$

$$(d) \overline{A+B+C} = \overline{A} + \overline{B} + \overline{C}$$

S'09 : 6 FN : EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum Marks : 100*

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Group A

1. (a) Draw the circuit diagram for fixed bias considering an $n-p-n$ transistor in the CE configuration. Derive the expressions for its stability factors. 10
- (b) Distinguish between CE, CB and CC modes of operation of a transistor. 4
- (c) What is the Darlington connection? Compare between an emitter follower and a Darlington pair. 3+3

(Turn Over)

2. Draw the circuit diagram of a two stage RC coupled CE transistor amplifier and explain its operation.
Obtain an expression for the voltage gain of the RC-coupled amplifier in the mid and high frequency ranges. Write down the assumptions as may be necessary for the derivation. 20
3. (a) What is negative feedback to an amplifier? Show that negative feedback can change the input and output impedances of an amplifier. 2+6
- (b) Give the circuit diagram of a Hartley oscillator and explain its operation. 8
- (c) Discuss the principle of operation of a crystal oscillator. 4
4. (a) How do the characteristics of a practical op-amp differ from those of the ideal op-amp. 4
- (b) Draw the gain frequency response of an op-amp operating in open loop mode and explain how it can be changed using feedback. 2+6
- (c) With a neat circuit, explain how an op-amp can be used to add three voltages—2 V, 3 V and 4 V. 8

Group B

5. (a) Convert the decimal number $(36.0625)_{10}$ to binary. 5
- (b) Find the hexadecimal equivalent of the number $(41801.225)_{10}$. 6

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(2)

(Continued)

- (c) Prove the following Boolean identities: 3 × 3

(i) $A + B[AC + (B + \bar{C})D] = A + BD$

(ii) $AB + AC + B\bar{C} = AC + B\bar{C}$

(iii) $(A + B)(B + C)(C + A) = AB + BC + CA.$

6. (a) What do you understand by 'minterm' and 'maxterm'? Discuss. 4

- (b) Simplify the function F by Karnaugh's reduction technique, where

$$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D}$$

Realize the simplified expression using NAND gates. 10

- (c) Realize the following gates using only NOR gates: 3+3

(i) Two input AND gate.

(ii) Exclusive-OR gate.

7. (a) Draw the circuit diagram and explain operation of a two input TTL NAND gate. What is totempole output and why is it provided? 8
- (b) Differentiate between a latch and a flip-flop. 4
- (c) Realize JK flip-flop using SR flip-flop. Give the realization diagram. Also, explain the problem of race related to these flip-flops. 5+3
8. (a) Distinguish between multiplexer and demultiplexer, using appropriate diagrams. Discuss the principle of operation of an 8 input multiplexer. 5+5

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(3)

(Turn Over)

- (b) With a neat circuit, explain the operation of a successive approximation type A/D converter. Mention some of its advantages and disadvantages. 10

Group C

9. Choose the correct answer for the following: 10 × 2

- (i) Barkhausen criteria for sustained oscillation is

- (a) $-A\beta = 1$
 (b) $A\beta = 0$
 (c) $A\beta = 1$
 (d) $A = 1/\sqrt{\beta}$

- (ii) The maximum theoretical conversion efficiency of a class A transformer coupled amplifier is

- (a) 15%
 (b) 25%
 (c) 50%
 (d) 78.5%

- (iii) Efficiency of a half wave rectifier is

- (a) 40.6%
 (b) 20.3%
 (c) 81.2%
 (d) 60.9%

- (iv) One of the following is not the characteristic of an ideal op-amp:

- (a) Infinite voltage gain
 (b) Infinite input impedance
 (c) Infinite bandwidth
 (d) Infinite offset voltage

- (v) Presence of emitter bypass capacitor adversely affects the

- (a) low frequency response.
 (b) medium frequency response.
 (c) high frequency response.
 (d) complete frequency range.

- (vi) Which one of the following Boolean algebra rule is correct?

- (a) $A \cdot \bar{A} = 1$
 (b) $A + AB = A + B$
 (c) $A + \bar{A} \cdot B = A + B$
 (d) $A(A + B) = B$

- (vii) The excess-3 code is also known as

- (a) weighted code
 (b) cyclic redundancy code
 (c) self-complementing code
 (d) algebraic code

(viii) Which one of the following is not a sequential circuit ?

- (a) flip-flop
- (b) counter
- (c) shift register
- (d) multiplexer

(ix) Which one of the following counters has the highest speed ?

- (a) Asynchronous counter
- (b) Synchronous counter
- (c) Ripple counter
- (d) Ring counter

(x) The functional difference between SR and JK flip-flops is that

- (a) JK flip-flop has a feedback path.
- (b) JK flip-flop does not require any external clock pulse.
- (c) JK flip-flop is faster than SR flip-flop.
- (d) JK flip-flop can accept both inputs.

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Group A

1. (a) What are the two main biasing techniques commonly used in BJT circuits? Draw the related circuit diagrams and explain how the biasing is effected. 4
- (b) How is the biasing done in the case of FET? Explain utility of the load line and the bias line in FET circuits. 6
- (c) A CE transistor circuit has a current gain β of 60. The collector supply voltage is 20 V. If $R_c = 10\text{ K}$, $R_e = 100\ \Omega$ and a resistance of $1\text{ M}\Omega$ is connected from V_{CC} to the base, calculate the collector current (take $V_{BE} = 0.6\text{ V}$). 10

2. (a) What are multistage amplifiers and where are they used? Draw a set of n -cascaded amplifiers and show that the overall voltage gain A_V can be expressed as

$$A_V = A_{V_1} A_{V_2} A_{V_3} \dots A_{V_n}$$

where A_V 's denote voltage gains of individual stages. Can this value of n be increased indefinitely? Give reasons for your answer. 6

- (b) In a CE R-C coupled amplifier, the total effective shunt capacitance in the input circuit, including the Miller effect component, is 300 pF. The hybrid π -parameter $r_{b'e} = 800 \Omega$. Calculate the upper 3 dB frequency. At what frequency in the high frequency range will the voltage gain be below 6 dB of the mid-band gain? 7 + 7
3. (a) How can you convert an amplifier into an oscillator? Explain the operation of an R-C phase-shift oscillator. 2 + 4
- (b) Draw the circuit diagram of a Wien bridge oscillator and explain its operation. Prove that the condition of oscillation in this case requires that the feedback factor $\beta = -1/\delta$, where δ is a number greater than 3. 14
4. (a) What is a differential amplifier and how it can be realized using an op amp.? Draw the circuit diagram of a symmetrical emitter coupled difference amplifier and explain its operation. Re-draw this circuit incorporating a constant current source and state its advantages. 10

- (b) A differential amplifier has a CMRR $\rho = 1000$. Let the first set of inputs be $v_1 = +100 \mu\text{V}$ and $v_2 = -100 \mu\text{V}$; the second set of inputs are $v_1 = 1100 \mu\text{V}$ and $v_2 = 900 \mu\text{V}$. Calculate the percentage difference in the output voltage obtained in the two cases. 10

Group B

5. (a) Write a brief account of the binary, octal and hexadecimal number system. How can you convert a decimal fraction into its binary equivalent? Explain with an example. 6
- (b) What does BCD stand for? How can you convert a BCD number to its decimal equivalent? 6
- (c) Convert directly the following: (i) $(3578)_8$ to $(X)_2$, and (ii) $(1011.01101)_2$ to $(X)_8$. 8
6. (a) What is the difference between basic logic gates and universal logic gates? Show how you can obtain an OR and an AND gate using NOR gates. 8
- (b) Establish the following Boolean identities: 3 + 3
- (i) $(A + \underline{BC}) = (A + B)(A + C)$.
- (ii) $A + \underline{AB} = A + B$
- (c) State and prove De Morgan's theorem. What is its utility? 6
7. (a) What are adder circuits and what are the functions of half-adder and full-adder? Draw the logic circuit of a full-adder alongwith its truth table and explain its operation. 10

- (b) Draw the circuit of an eight bit adder-subtractor with a sub-signal and explain how the circuit can perform binary operations. 10
8. (a) What are flip-flops and why are they called by this name? Explain the operation of an S-R flip-flop and show why an ambiguity arises for $S = R = 1$. 8
- (b) How can you convert an S-R flip-flop to a J-K flip-flop? Draw the related circuit diagram and show how the race-condition is avoided in a J-K flip-flop. 8
- (c) What is a J-K master-slave flip-flop and what is its advantage? 4

Group C

9. Choose the *correct* answer for the following : 10×2
- (i) Which biasing technique of a BJT uses one resistor?
- (a) self-bias
(b) emitter-bias
(c) fixed-bias
(d) None of the above.
- (ii) The stability factor, S' , for a transistor circuit is equal to
- (a) R_e
(b) $-1/R_e$
(c) $-R_e$
(d) $-1/(R_e + R_c)$

(iii) Which one of the following is not an element of a hybrid- π model of a CE transistor circuit?

- (a) $r_{bb'}$
(b) C_c
(c) C_e
(d) h_{fe}

(iv) Which circuit has a voltage gain $A_v = +1$?

- (a) CE
(b) CB
(c) CC
(d) CE followed by CB

(v) The emitter follower circuit is a case of which type of feedback?

- (a) voltage series
(b) current series
(c) voltage shunt
(d) current shunt

(vi) Maximum possible conversion efficiency of a class-B amplifier is

- (a) 25%
(b) 50%
(c) 75%
(d) 78.5%

- (vii) A three-input OR gate has output equal to 0 when
- (a) all its inputs are high.
 - (b) two of its inputs are high.
 - (c) all are low.
 - (d) one is high and the other two are low.
- (viii) For standard TTL, the logic 0 has a voltage level between
- (a) 0 and 1 V
 - (b) 0 and 0.8 V
 - (c) 0 and 0.5 V
 - (d) 0 and 0.4 V
- (ix) The purpose of a Schmitt trigger circuit is to generate a
- (a) triangular wave
 - (b) saw-tooth wave
 - (c) sinusoidal wave
 - (d) square wave
- (x) An astable multivibrator is also called
- (a) free-running.
 - (b) edge-triggered.
 - (c) emitter-coupled.
 - (d) multi.

S'10 : 6 FN : EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum marks : 100*

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

*All parts of a question (a, b, etc.) should be
answered at one place.*

*Answer should be brief and to-the-point and be supple-
mented with neat sketches. Unnecessary long answers
may result in loss of marks.*

*Any missing or wrong data may be assumed suitably
giving proper justification.*

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Show that the value of transconductance, g_m , for a FET biased at I_{DQ} is lower than the value of g_m for a BJT biased at $I_{CQ} = I_{DQ}$. 5
- (b) Explain why the quiescent collector current must be essentially independent of variations in β to achieve bias stabilisation. 5
- (c) In a four-resistor bias network $V_{cc} = 28\text{ V}$, $R_c = 6.8\text{ k}\Omega$, $R_E = 1.2\text{ k}\Omega$, $R_1 = 90\text{ k}\Omega$ and $R_2 = 10\text{ k}\Omega$. Determine the Q point assuming that $I_{CQ} = 0$ and $\beta = 60$. 5

- (d) Explain how the four-resistor bias network tends to minimise variations in I_{DQ} caused by unit-to-unit changes in the FET. 5
2. (a) Draw a neat sketch showing the variation of hybrid parameters h_{ib} , h_{rb} , h_{fb} and h_{ob} with emitter current. 5
- (b) Show that the voltage gain of a CS amplifier is given by $A_V = -\mu R_D / (r_d + R_D)$ 5
- (c) How do coupling and bypass capacitors affect the frequency response of an amplifier stage? 4
- (d) For the condition that
 $(1 + \beta) R_E \gg R_S + r_\pi$
 show that the voltage gain of a common emitter stage with emitter resistance is essentially independent of β and approaches $-R_C/R_E$. 6
3. (a) Explain the meaning of frequency distortion, amplitude distortion and phase distortion with the help of suitable examples. 5
- (b) A multistage amplifier comprises N identical stages and has a cut-off frequency of ω_0 . Show that the upper band limit ω_2 of each stage is given by

$$\omega_2 = \omega_0 / \sqrt{2^{1/N} - 1}$$
 5
- (c) Sketch the normalised step response of a low-pass circuit and define rise time. For an amplifier, with 1 MHz bandpass, determine the rise time. 5
- (d) Define tilt or sag. It is desired to pass a 50Hz square wave with less than 10 percent sag. Determine the largest permissible value of the lower 3 dB frequency. 5
4. (a) Explain how temperature stability of an amplifier gets modified by negative feedback. 4
- (b) Draw the circuit diagram of a Wien bridge oscillator and derive an expression for the frequency of oscillation. 6
- (c) Using an op amp, draw the circuit diagram of non-inverting integrator and derive all expression for the output in terms of the input. 4
- (d) Show that the maximum conversion efficiency of an idealised class B push-pull circuit is 78.5 per cent. 6
- Group B**
5. (a) Find the decimal, octal and hexadecimal equivalents of the decimal number 73. 4
- (b) Show that a positive logic OR gate is the same as a negative logic AND gate. 6
- (c) State De Morgan's law and design a logic $Q = AB + \overline{AB} C$. 4
- (d) Minimise the following switching function on a Karnaugh map:
 $F = \sum (3, 7, 11, 12, 13, 14, 15) + \sum_4 (0, 4)$. 6
6. (a) Write the truth table for a full subtractor. 4
- (b) Implement a half adder using only NOR gates. 6
- (c) Draw and explain the circuit diagram of a MOS inverter. 6
- (d) Discuss the relative merits of TTL and CMOS 4

7. (a) Derive the characteristic equation of a T flip-flop. 4
 (b) With reference to a Schmitt trigger, define LTP and UTP. 4
 (c) Show that the simple ring counter suffers from lockout. 6
 (d) Explain how a decade counter can be built using four flip-flops. 6
8. (a) Draw and explain a block diagram of circuitry for two registers X and Y of three flip-flops each so that either Y can be transferred to X or the 1s complement of Y can be transferred to X. 7
 (b) Describe the advantages and disadvantages of dynamic IC memories. 3
 (c) The basic step of a 9 bit D/A converter is 10.3 mV. Determine the output for an input of 101101111, given that 000000000 represents 0V. 4
 (d) Draw and explain the functional diagram of successive approximation A/D converter. 6

Group C

9. Choose the *correct* answer for the following: 10×2
- (i) The return difference of a feedback amplifier is given by
- (a) $-A\beta$
 (b) $+A\beta$
 (c) $1 - A\beta$
 (d) $1 + A\beta$

- (ii) For a feedback amplifier, the return ratio $T = 49$. If $\Delta T = +25$, the corresponding fractional change in the gain of the feedback amplifier is
- (a) 0.0068
 (b) 0.068
 (c) 0.25
 (d) 2.5
- (iii) The output of an op amp voltage follower is a triangular wave that changes from -3V to $+3\text{V}$ in $0.25\ \mu\text{s}$ when the input is a square wave of frequency 2 MHz and 8 V peak-to-peak amplitude. The slew rate of the op amp is
- (a) $8\ \text{V}/\mu\text{s}$
 (b) $24\ \text{V}/\mu\text{s}$
 (c) $7\ \text{V}/\mu\text{s}$
 (d) $4\ \text{V}/\mu\text{s}$
- (iv) A non-inverting amplifier with a gain of 100 is nulled at 25°C . The op amp offset voltage drift is $0.15\ \text{mV}/^\circ\text{C}$. At 50°C , the output voltage of the non-inverting amplifier is
- (a) 3.75 mV
 (b) 7.5 mV
 (c) 37.5 mV
 (d) 375 mV

(v) The ripple factor of a half wave rectifier is

- (a) 121%
- (b) 100%
- (c) 48.3%
- (d) 25%

(vi) An example of a self-complementing code is

- (a) 8421 code
- (b) Gray code
- (c) 7421 code
- (d) Excess-3 code

(vii) The idempotent law of Boolean algebra says that

- (a) $x + 1 = 1$
- (b) $x + x = x$
- (c) $x + xy = x$
- (d) $x(x + y) = x$

(viii) In order to build a MOD 18 ripple counter, the minimum number of flip-flops needed is equal to

- (a) 18
- (b) 9
- (c) 5
- (d) 4

(ix) A PLA (programmable logic array) has 16 inputs, 8 outputs and a total of 48 partial products. This PLA is referred to as a

- (a) $16 \times 48 \times 8$ PLA
- (b) $16 \times 8 \times 48$ PLA
- (c) $8 \times 16 \times 48$ PLA
- (d) $48 \times 16 \times 8$ PLA

(x) The input binary number to a 2 bit D/A converter is 10. The output of the D/A converter ranges from 0V to 10V. The output voltage of the D/A converter is equal to

- (a) 2.5 V
- (b) 5 V
- (c) 7.5 V
- (d) 10 V

W' 10 : 6 FN : EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum Marks : 100*

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

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answered at one place.*

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mented with neat sketches. Unnecessary long answers
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Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Is the operating point of a transistor amplifier fixed? If not, what are the factors responsible for its shift? 4
- (b) What is a load line? Explain its significance. 4
- (c) A Ge-transistor with $\beta = 49$ has the self-biasing arrangement, with $V_{cc} = 10\text{V}$, $R_L = 1\text{k}\Omega$, $V_{CE} = 5\text{V}$, $I_C = 4.9\text{mA}$; and $V_{BE} = 0.2\text{V}$. The stability factor, S , is desired to be 10. Obtain the value of R_1 , R_2 and R_e . 8
- (d) Distinguish between *CE*, *CB* and *CC* modes of operation of a transistor. 4

Group B

2. (a) With a neat schematic, explain the operation of a class B push-pull amplifier and prove that its efficiency is 78.5%. 4+6
- (b) Using h -parameter analysis, explain why gain falls at low frequency but remains constant at mid-frequency range if operation of an R-C coupled amplifier. 10
3. (a) Draw the equivalent circuit of an op-amp and write the characteristics of an ideal op-amp. 3+3
- (b) An amplifier using an op-amp with a slew rate of $1\text{ V}/1\ \mu\text{s}$ has a gain of 40 dB. If this amplifier has to faithfully amplify sinusoidal signal from d.c. to 20 kHz without introducing any slew rate induced distortion, calculate the maximum input signal voltage. 6
- (c) Design a circuit using op-amp, which can add three input voltages of 2 V, 4 V and 6 V, and also explain how this circuit can be modified to get the output of the op-amp as an average of these three input voltages. 8
4. (a) Write the condition for oscillation in an oscillator circuit. How can oscillators be classified? 4
- (b) With a neat schematic, explain the operation of a Colpitt oscillator. Mention its drawback and explain how it can be overcome in Hartley oscillator. 6+2
- (c) Calculate the ripple factor of a full wave rectifier. Explain how ripples can be minimized by using L-type filter. 5+3

5. (a) Prove that $\overline{AB + BC + CA} = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}$. 4
- (b) Represent $(-16)_{10}$ in sign magnitude, 1s complement and 2s complement representation. 2
- (c) Simplify the following using K -map:

$$f(A, B, C, D) = \sum m(7, 8, 9) + \sum d(10, 11, 12, 13, 14, 15)$$
 10
- (d) What do you understand by 'minterm' and 'maxterm'? Discuss? 4
6. (a) Explain the following terms applicable to digital IC: 4 × 1
- (i) Propagation delay time
- (ii) Figure of merit
- (iii) Noise immunity
- (iv) Fan-out.
- (b) Draw the circuit diagram and explain the operation of a CMOS inverter. Mention its advantages over other logic gates. 6+2
- (c) Design a gray code to BCD converter, and draw its logic diagrams. 8
7. (a) Discuss how a JK flip-flop can be constructed using a clocked SR flip-flop. Depict a table showing the excitation requirements of JK flip-flop. 10
- (b) Design a modulo-5 synchronous counter. Draw the state diagram of the modulo-5 counter and show the state table for the counter. 10

8. (a) Explain the function of a dual slope type analog-to-digital converter. Prove that the count recorded by its counter is equal to amplitude of the analog voltage. 8
- (b) Design the circuit of an astable multivibrator using IC-555 and find out an expression for its time period $T = 0.69 (R_A + 2R_B) C$. 8
- (c) What are programmable logic arrays? 4

Group C

9. Choose the *correct* answer for the following: 10×2
- (i) Decimal 43 in hexadecimal and BCD number system is respectively
- (a) B2, 01000011
- (b) 2B, 01000011
- (c) 2B, 00110100
- (d) B2, 01000100
- (ii) The minimum number of 2 line to 1 line MUX required to realize a 4 line to 1 line MUX is
- (a) 1
- (b) 2
- (c) 3
- (d) 4
- (iii) The minimum number of comparators required to build an 8 bit flash ADC is
- (a) 8
- (b) 63
- (c) 255
- (d) 256

- (iv) How many 32×1 RAM chips are needed to provide a memory capacity of 256 K bytes?
- (a) 8
- (b) 32
- (c) 64
- (d) 128
- (v) $(C012.25)_{16} - (10111001110.101)_2$ is
- (a) $(135103.412)_8$
- (b) $(564411.412)_8$
- (c) $(564411.205)_8$
- (d) $(135103.205)_8$
- (vi) An ideal op-amp is an ideal
- (a) voltage controlled current source.
- (b) voltage controlled voltage source.
- (c) current controlled current source.
- (d) current controlled voltage source.
- (vii) If the differential voltage gain and common mode voltage gain of a differential amplifier are 48 dB and 2 dB, respectively, then its common mode rejection ratio is
- (a) 23 dB
- (b) 25 dB
- (c) 46 dB
- (d) 50 dB

- (viii) The effect of current shunt feedback in an amplifier is to**
- (a) increase the input resistance and decrease the output resistance.**
 - (b) increase both input and output resistance.**
 - (c) decreases both input and output resistances.**
 - (d) decrease the input resistance and increases the output resistance.**
- (ix) Efficiency of a full-wave rectifier is**
- (a) 40.6%**
 - (b) 121%**
 - (c) 48%**
 - (d) 81.2%**
- (x) Generally the gain of a transistor amplifier falls at high frequencies due to the**
- (a) internal capacitance of the device.**
 - (b) coupling capacitor at the input.**
 - (c) skin effect.**
 - (d) coupling capacitor at the output.**

S'11 : 6 FN : EC 406 (1481)

ELECTRONIC CIRCUITS*Time : Three hours**Maximum Marks : 100*

Answer FIVE questions, taking ANY TWO from Group A, ANY TWO from Group B and ALL from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answers may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Give the biasing techniques commonly used in biasing BJT in CE configuration. For the circuit shown in Fig. 1, calculate the d.c. value of V_{CE} (take $\beta = 60$) and cut-in voltage of emitter-base diode as 0.6 V. 6 + 10

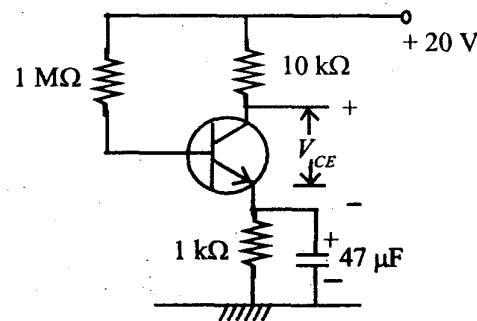


Fig. 1

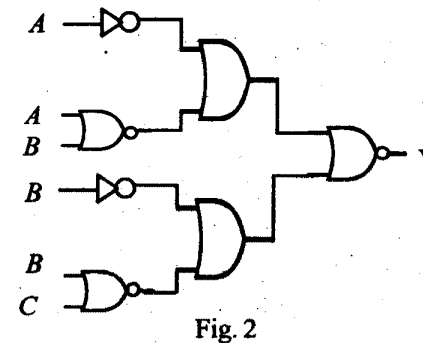
(Turn Over)

- (b) Briefly mention the stability factors S , S' and S'' . Hence, show how they can be used in minimizing the variation ΔI_c of collector current. 4
2. (a) Enunciate various types of feedback used in electronic circuits. Show that the gain, A_f , of an amplifier with feedback is related to the gain A without feedback by the relation, $A_f = A/(1 + A\beta)$, where β is the feedback factor. Does this equation represent a positive or negative feedback? 6 + 4
- (b) Draw the circuit diagram of an emitter follower and explain its operation. Hence, prove that this circuit represents a case of voltage series negative feedback. 4 + 6
3. (a) Explain the terms 'gain A_d for different mode signal' and 'gain A_c for common mode signal' as applied to a differential amplifier. For a differential amplifier derive CMRR. Should it be high or low? Give reasons for your answer. 4 + 4
- (b) A symmetrical emitter-coupled differential amplifier has $R_c = 5 \text{ k}\Omega$, $R_e = 4 \text{ k}\Omega$ and $R_s = 5 \text{ k}\Omega$. Each of the two identical transistors has $h_{fe} = 50$ and $h_{ie} = 1100 \Omega$. Calculate A_c and A_d for this circuit. 12
4. (a) Draw the circuit diagram of a class A transformer coupled power amplifier and obtain an expression for its power output in terms of maximum and minimum values of current and voltage. Hence, show that the maximum efficiency obtainable from this circuit is 50%. 4 + 6

- (b) A class B push pull amplifier has $V_{cc} = 20 \text{ V}$, $N_2 = 2N_1$ (turns ratios) and $R_L = 8 \Omega$. Input to the amplifier is sinusoidal, $V_{min} = 4 \text{ V}$. Determine the output signal power, input d.c. power, percent collector, circuit efficiency, and collector dissipation per transistor. 10

Group B

5. (a) Briefly explain four main number systems used in digital electronics. Hence, show the process you would follow in order to transform a decimal fraction to its binary equivalent. 4
- (b) Transform the following: 4 x 4
- (i) $(367.52)_8 = ()_2$
 (ii) $(110101.101010)_2 = ()_8$
 (iii) $(1011011011)_2 = ()_{16}$
 (iv) $(4BAC)_{16} = ()_2$
6. (a) Draw the simplest possible logic diagram that implements the output Y of the logic diagram shown in Fig. 2. 10



- (h) Reduce, using K-map, the expression $\sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ and implement it in universal logic. 10
7. (a) What are edge-triggered flip-flops and in what respect are they different from ordinary flip-flops? Draw the logic symbol of a positive and negative edge-triggered S-R flip-flops and explain their operation on the basis of their truth-table. 8
- (b) Explain the operation of a monostable multi-vibrator using a NOR gate and an inverter. Realize the same circuit using NAND gates. Show also the trigger inputs and pulse output. 12
8. Write short notes on *any two* of the following : 10 + 10
- (a) CMOS circuits
- (b) Ripple and synchronous counters
- (c) D/A and A/D converters.
- Group C**
9. Choose the *correct* answer for the following : 10 × 2
- (i) The base-to-emitter voltage, V_{BE} , in a transistor in forward bias decreases with increase in temperature at the following rate :
- (a) 25 mV/°C
- (b) 0.25 V/°C
- (c) 2.5 mV/°C
- (d) 0.6 mV/°C
- (ii) In a JFET, transconductance, g_m , is of the order of
- (a) 1 ms
- (b) 100 ms
- (c) 1 s
- (d) 100 s
- (iii) If f_L^* and f_H^* are the lower and upper 3 dB frequencies, respectively of a set of cascaded amplifiers with f_L and f_H , the corresponding values of individual stages, then
- $$[(f_H^* / f_H) \times f_L^* / f_L]$$
- is equal to
- (a) 0
- (b) 1
- (c) 2^{n-1}
- (d) $\sqrt{2^n - 1}$
- where n is the number of stages.
- (iv) FET phase shift oscillator uses
- (a) voltage series feedback.
- (b) voltage shunt feedback.
- (c) current series feedback.
- (d) current shunt feedback.
- (v) The gain-bandwidth product of 741 op-amp is about
- (a) 0.1 MHz
- (b) 1 MHz
- (c) 10 MHz
- (d) 100 MHz

(vi) Which theorem gives the following identity ?

$$AB + \bar{A}C = (A + C) (\bar{A} + B)$$

- (a) De Morgan's
- (b) Transposition
- (c) Consensus
- (d) None of the above.

(vii) A 16-square on a K-map eliminates how many variables ?

- (a) 4
- (b) 8
- (c) 6
- (d) 3

(viii) To form a half-adder, which two gate combinations are essential ?

- (a) AND and OR
- (b) AND and NOR
- (c) AND and XOR
- (d) AND and NOT

(ix) What is the other name of a Johnson counter ?

- (a) Ring counter
- (b) Ripple counter
- (c) Up-down counter
- (d) Twisted-ring counter

(x) A D/A converter has 10 V full scale (maximum) output voltage and an accuracy of $\pm 0.2\%$. Then the maximum error for any output voltage is

- (a) 10 mV
- (b) 20 mV
- (c) 50 mV
- (d) 100 mV.

W'11:6 FN:EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum Marks : 100*

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

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answered at one place.*

*Answer should be brief and to-the-point and be supple-
mented with neat sketches. Unnecessary long answers
may result in loss of marks.*

*Any missing or wrong data may be assumed suitably
giving proper justification*

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Determine the values of R_1 and R_2 in a CE amplifier with voltage divider bias, where the emitter resistance $R_e = 100 \Omega$, $V_{CC} = 12 \text{ V}$, $I_B = 0.3 \text{ mA}$, $\beta = 100$ and stability factor $S (\cong R'_B / R_e)$. The quiescent point is set at $V_{CE} = 4.25 \text{ V}$ for $I_C = 18 \text{ mA}$. Give a suitable sketch with your answer to show the complete circuit. 4 + 4 + 4

- (b) Give the h-parameter model of a transistor suitable for small analysis at low frequency with the help of a suitable sketch. Define the terms h_{ie} , h_{oe} , h_{fe} and h_{re} with the known signals i_c , i_b , v_c and v_b . Assume CE configuration for the transistor. 8

2. (a) Estimate the current gain (A_i), voltage gain (A_v), voltage gain with R_s (AV_s), input resistance (R_i) and output resistance R_o for a common collector bipolar transistor. Why is it also called an emitter follower? Suggest some applications of an emitter follower. 6 + 2 + 2
- (b) Design a common source amplifier with current mirror load and estimate its transconductance (g_m) and output impedance (R_o) from its small signal equivalent. 10
3. (a) Name the types of amplifiers (A) topologically involved in voltage-series, voltage-shunt, current-series and current-shunt feedback configuration and justify your answer analytically. 4 × 2
- (b) What are the advantages of –ve feedback? Define desensitivity (D) and give mathematical expression for amount of feedback (N) in decibels in terms of D . 2 + 2
- (c) Using approximate hybrid- π model for a single-stage CE amplifier at high frequency, find the expression for current gain (A_i) and f_T which is the frequency at which $|A_i| = 1$. 4 + 4
4. (a) Design a non-inverting summing amplifier using a single op-amp and give the analysis. Derive an expression for the input resistance of the amplifier designed as above. 4
- (b) Define (i) phase margin, and (ii) gain margin. 2 + 2

- (c) State the Barkhausen criteria for setting up of an oscillation and its sustenance. Describe function of a phase shift oscillation using op amp. 2 + 2
- (d) Where is the operating point located in a class B amplifier and what is the efficiency η achievable for this type of amplifier? Is class B amplifier efficiency more than that of class A. Give the expression for η and show the operating point with a suitable sketch. What is class AB operation? 3 + 3 + 2

Group B

5. (a) Simplify using Karnaugh map: 5 + 5
- (i) $F(A, B, C, D) = \Sigma(0, 1, 2, 3, 4, 8, 12)$
- (ii) $F(A, B, C, D) = \Pi(1, 3, 4, 6, 9, 11, 12, 14)$
- (b) State the De Morgan's theorem and prove it for two variables x and y . Also, prove that $x + \overline{xy} = 1$. 2 + 2
- (c) Using distributive law, simplify the following without doing multiplication: 6
- $$F = (A + B + C + D)(A + B + C + E)(A + B + C + F)$$
6. (a) Give the truth table of (i) full adder, and (ii) half subtractor. Give the logic realization using 2-input AND, OR and INVERTER gates. 3 + 3 + 4 + 4
- (b) Give the logic realisation of J-K master slave clocked flip-flop using NAND and inverter gates. 6

7. (a) Design a CMOS-inverter and explain how it operates with the help of a suitable sketch. Justify the d.c. bias conditions in it. 5
- (b) Design and explain the operation of a three-input TTL-NAND with a suitable sketch. 5 + 10
8. Write short notes on *any two* of the following : 10 + 10
- (a) R-2R ladder DA converter
 (b) 4-bit ripple counter
 (c) Dynamic RAM and refresh cycle

Group C

9. (A) Choose the *correct* answer for the following : 8 × 2
- (i) If $\alpha (= I_C / I_E)$ is changed from 0.9 to 0.99, what will be the % change in $\beta (= I_C / I_B)$?
- (a) 10%
 (b) 100%
 (c) 1000%
 (d) 9.9%
- (ii) While BJT is a ——— controlled device, MOS is a ——— controlled device.
- (a) minority carrier ; majority carrier
 (b) current ; voltage
 (c) charge ; electron
 (d) majority carrier ; minority carrier

- (iii) If an amplifier has a gain (A) = 10000 in absolute terms, what would be the gain (A) in dB.
- (a) 40 dB
 (b) 80 dB
 (c) 40 dBm
 (d) 80 dBm
- (iv) If power dissipation of a class AB push-pull amplifier increases by 3 dBm, by how much does it increase in absolute terms ?
- (a) 3 mW
 (b) 1000 mW
 (c) 2 mW
 (d) 2000 mW
- (v) Static RAM is ——— than dynamic RAM which requires periodic ——— for charge retention.
- (a) more compact ; heating
 (b) simpler ; cleaning
 (c) slower ; clocking
 (d) faster ; refreshing
- (vi) Design of CLA would need
- (a) design of code converter and counter.
 (b) design of J-K and T flip-flops.
 (c) design of generate and propagate terms.
 (d) design of sequential circuits and combinational circuits.

(vii) How many MOS devices would be needed at the minimum to design a three-input and a two-input AND using standard CMOS-logic?

- (a) 8 and 8
- (b) 4 and 6
- (c) 6 and 3
- (d) 6 and 6

(viii) Karnaugh map uses — code because only — change is allowed between two consecutive square squares for simplification.

- (a) gray ; one-bit
- (b) ASCII ; two-bit
- (c) hex ; one-bit
- (d) octal ; one bit

(B) Select the *correct* option for the following : 4×1

(i) The MOS equivalent of common collector amplifier is

- (a) Common drain amplifier
- (b) Emitter follower amplifier
- (c) Common gate amplifier
- (d) Common source amplifier

(ii) For an amplifier to be stable, the poles must lie on the

- (a) right half of the S-plane.
- (b) on the positive X-axis.
- (c) on the negative X-axis.
- (d) left half of the S-plane.

(iii) What is the octal equivalent of FF_{16} ?

- (a) 255
- (b) 377
- (c) 256
- (d) 1111111

(iv) How many 2-input NAND gates at the minimum would you need to design a 2-input Ex-OR ?

- (a) 3
- (b) 4
- (c) 5
- (d) 6

W'12: 6 FN: EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum Marks : 100*

Answer FIVE questions, taking ANY TWO from Group A, ANY TWO from Group B and ALL from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answer may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification.

Figures on the right-hand side margin indicate full marks

Group A

1. (a) With a neat circuit, explain the operation of a self-bias circuit for an N-P-N transistor. Also, derive the way instability is reduced by such a bias. 6 + 6
- (b) Draw the h-parameter equivalent circuit of a bipolar junction transistor operating in the CE mode. Find an expression for its current gain and output resistance. 2 + 6
2. (a) With a neat circuit diagram, explain the operation of a two identical gain stage R-C coupled amplifier. Draw its gain-frequency response. Explain, using high frequency model analysis, why gain is constant over mid-frequency range and falls at low frequency region of operation. Derive an expression for overall bandwidth. 4 + 2 + 6

(Turn Over)

- (b) Mention the effect of negative feedback in amplifier circuit. Also, prove that negative feedback increases the input impedance and bandwidth of an amplifier. 2 + 6
3. (a) With a neat circuit, explain the operation of a Colpitt oscillator. Find an expression for its frequency of oscillation and condition for sustained oscillation. Also, write the drawback of this circuit and explain how it can be overcome in Hartley oscillator. 4 + 8 + 2
- (b) Explain working of a bridge rectifier. Calculate the efficiency and ripple factor of a bridge rectifier circuit. 6
4. (a) Draw the functional block diagram of an op amp and mention the function of each block. 6
- (b) Draw the gain frequency response of an op amp operating in open-loop mode. How negative feedback improves this gain frequency response of the op amp? 2 + 4
- (c) Design a circuit using op amp non-inverting integrator, which can add three voltages of 3V, 4V and 5V and the result at its output is integration of the sum. 4
- (d) Design a circuit using op amp, which can solve the following second order differential equation : 4
- $$4\ddot{x} - 3\dot{x} + 5x = 4$$

Group B

5. (a) What is BCD code? Write its advantages and disadvantages over straight binary code. Design a BCD encoder-decoder system. 2 + 2
- (b) State and prove de-Morgan's theorem and using the theorem, simplify the following expression : 4 + 2

$$Y = \overline{AB + A + AB}$$

- (c) Design a grey to binary code converter by using minimum number of gates. 6
- (d) Prove that NAND and NOR gates are universal logic gates. Design a NOR gate using emitter coupled logic. 4
6. (a) Simplify the following function using K-map and draw the logic gate realization of the corresponding circuit: 7
- $$f = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$$
- (b) Draw the 'Totem Pole' configuration of TTL NAND gate and explain its operation. 8
- (c) Derive truth table of a full subtractor and obtain the expression for difference and borrow. 5
7. (a) Describe a D-flip-flop with master-slave stages. How does it differ from a T-flip-flop? Mention their specific application. Also, explain, with a necessary circuit, that how T-type flip-flop can be realized from an S-R flip-flop. 4 + 1 + 3
- (b) Design an asynchronous counter using J-K flip-flop to count in the random sequence 0, 1, 3, 2, 5, 6, 0, 1, 3, Compare its merits with that of synchronous counter. 8
- (c) Differentiate between a latch and a flip-flop. What do you mean by positive edge trigger flip-flop? 4
8. (a) Draw the circuit of a monostable multi-vibrator and explain its operation. Find an expression for its time period. Where does it find application in clock generation? 6 + 2

- (b) With a necessary circuit, explain the operation of a binary weighted resistor-type digital-to-analog (D/A) converter. Write its drawback. What do you mean by R-2R logic? 7 + 1
- (c) Write a short technical note on Schmitt trigger. How can it be made to oscillate? 4

Group C

1. Choose the *correct* answer for the following: 10 × 2

- (i) One of the following is not the characteristic of an ideal op amp:
- (a) Infinite voltage gain
 - (b) Zero offset voltage
 - (c) Infinite bandwidth
 - (d) Zero slew rate.
- (ii) In a 255 bit flash type A/D converter, total number of comparators required is
- (a) 8
 - (b) 7
 - (c) 6
 - (d) 5
- (iii) Basic building block of an R-S flip-flop is
- (a) a monostable multivibrator.
 - (b) a bistable multivibrator.
 - (c) an astable multivibrator.
 - (d) a Schmitt trigger.

- (iv) The logic family, which has the maximum speed of operation, is
- (a) PL
 - (b) ECL
 - (c) TTL
 - (d) CMOS
- (v) A mod -10 counter requires following number of flip-flops for its design:
- (a) 3
 - (b) 4
 - (c) 5
 - (d) 6
- (vi) A 4-bit ripple counter can count
- (a) 4 clock pulses.
 - (b) 8 clock pulses.
 - (c) 16 clock pulses.
 - (d) 32 clock pulses.
- (vii) Berkhausen criterion for sustain oscillation in an oscillator circuit, the loop gain is
- (a) $|AB| = 1$
 - (b) $|AB| = 0$
 - (c) $AB = 1$

(d) $AB = 0$

(viii) One of the following is a self-complementary code :

(a) 8421 code

(b) 7421 code

(c) Gray code

(d) Excess-3 code

(ix) The efficiency of class B push-pull amplifier is

(a) 25.4 %

(b) 50 %

(c) 78.5 %

(d) 91.2 %

(x) Crystal oscillators are superior to tuned LC oscillators mainly because of their

(a) smaller size.

(b) high Q value.

(c) availability.

(d) high degree of frequency stability.

S'13 : 6 FN : EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum Marks : 100*

Answer FIVE questions, taking ANY TWO from Group A, ANY TWO from Group B and ALL from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answer may result in loss of marks.

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Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Discuss the need for biasing a transistor. What do you mean by operating point? 2 + 2
- (b) Draw the collector to base feedback method for biasing a transistor and derive an expression for stability factor. 2 + 6
- (c) For a self-biased NPN silicon transistor, $\beta = 60$, $R_1 = 80 \text{ K}$, $R_2 = 10 \text{ K}$, $R_c = 5.7 \text{ K}$, $R_e = 1.1 \text{ K}$. If the supply voltage is 15 V, find the Q -point. 8
2. (a) Draw the h -parameter equivalent circuit of a transistor operating in CE mode. From the circuit, find an expression for input resistance and output resistance in terms of h -parameter. Also, write some of the limitations of h -parameter analysis. 2 + 6 + 2

- (b) Explain the operation of a class B push pull amplifier with a neat schematic. Prove that the efficiency is 78.5% for the amplifier. 4 + 6
3. (a) Draw the gain frequency response of an op amp, and explain with necessary derivation that gain falls at the rate of 20 dB/decade after cut-off. 1 + 5
- (b) Using an op amp, draw the circuit diagram of non-inverting differentiator and derive an expression for the output in terms of the input. 4
- (c) Show that the voltage gain of a CS amplifier is given by
- $$A_v = -\mu R_D / (r_d + R_D) \quad 5$$
- (d) A multistage amplifier comprises N identical stages and has a cut-off frequency w_0 . Show that the upper band limit w_2 of each stage is given by
- $$w_2 = w_0 / \sqrt{2^{1/N} - 1} \quad 5$$
4. (a) With a neat schematic, explain the operation of a bridge rectifier. Calculate its efficiency. 3 + 3
- (b) What is negative feedback to an amplifier? Show that negative feedback increases the stability and input impedance of an amplifier. 1 + 6
- (c) Write the conditions for oscillation in an oscillator circuit. Draw the circuit diagram of a Wein bridge oscillator and derive an expression for the frequency of oscillation. 1 + 6
- Group B**
5. Transfer the following : 3 × 2
- (i) $(123456)_8 = (?)_{16}$
- (ii) $(1101001101.1011)_2 = (?)_8$
- (iii) $(A75B)_{16} = (?)_8$
- (b) Simplify the following Boolean expression : 5 + 5
- (i) $(P + \bar{Q})(P.\bar{Q} + P.R)(\bar{P}.\bar{R} + \bar{Q})$
- (ii) $(A + B + C + D)(A + B + C + E)(A + B + C + F)$
- (c) Prove that a NAND gate is an universal logic gate. 4
6. (a) Draw and explain the operation of totem pole configuration of two-input TTL NAND gate. 8
- (b) Implement a half adder using only NAND gates. 6
- (c) Explain the operation of a CMOS inverter with a neat circuit. 6
7. (a) Minimize the following switching function on a Karnaugh map : 6
- $$Y = \sum m(3, 7, 11, 12, 13, 14, 15) + \sum d(0, 4)$$
- (b) How can an S-R flip-flop be modified into a J-K flip-flop? Explain the problem of 'Race' in a J-K flip-flop and how can it be overcome? 2 + 3 + 3
- (c) Explain, with a neat schematic, the operation of a ripple counter using three flip-flops. Write its truth table and draw its timing diagram. 6
8. (a) Explain the operation of a weighted resistor-type D/A converter with suitable circuit diagram. Mention its drawback. 6 + 2
- (b) Write a note on design of an astable multivibrator using a 555 timer. 6

- (c) Design a BCD to gray code converter and draw its logic diagram. 6

Group C

9. Choose the *correct* answer for the following : 10 × 2

- (i) The minimum number of 2 to 1 MUX required to realize a 4 to 1 MUX is

- (a) 1
(b) 2
(c) 3
(d) 4

- (ii) The minimum number of comparators required to build an 8-bit flash ADC is

- (a) 8
(b) 63
(c) 255
(d) 256

- (iii) Which one of the following is not a valid octal number ?

- (a) 777
(b) 875
(c) 222
(d) 111

- (iv) An example of a self-complementing code is

- (a) 8421 code
(b) Gray code
(c) 7421 code
(d) Excess-3 code

- (v) In order to design a Mod 12 counter, the number of flip-flops required is

- (a) 3
(b) 4
(c) 5
(d) 6

- (vi) The ripple factor of a half wave rectifier circuit is

- (a) 0.48
(b) 1.21
(c) 0.806
(d) 0.406

- (vii) The drain current of a MOSFET in saturation is given by $I_d = k(V_{GS} - V_T)^2$, where k is a constant. The magnitude of the transconductance, g_m , is

- (a) $\frac{k(V_{GS} - V_T)^2}{V_{DS}}$
(b) $2k(V_{GS} - V_T)$

$$(c) \frac{I_d}{V_{GS} - V_{DS}}$$

$$(d) \frac{k(V_{GS} - V_T)^2}{V_{GS}}$$

(viii) In a full-wave rectifier using two ideal diodes, V_{dc} and V_m are the d.c. and peak values of the voltage, respectively. If PIV is the peak inverse voltage, then appropriate relationship for this rectifier is

$$(a) V_{dc} = V_m/\pi ; PIV = 2 V_m$$

$$(b) V_{dc} = 2V_m/\pi ; PIV = 2 V_m$$

$$(c) V_{dc} = V_{dc}/\pi ; PIV = V_m$$

$$(d) V_{dc} = V_m/\pi ; PIV = V_m$$

(ix) The current gain of a BJT is

$$(a) g_m r_o$$

$$(b) g_m / r_o$$

$$(c) g_m r_\pi$$

$$(d) g_m / r_\pi$$

(x) One of the following is *not* the characteristic of an ideal op amp :

(a) Infinite voltage gain

(b) Infinite slew rate

(c) Zero input and output resistance

(d) Zero offset voltage

W' 13 : 6 FN : EC 406 (1481)**ELECTRONIC CIRCUITS***Time : Three hours**Maximum Marks : 100*

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

*All parts of a question (a, b, etc.) should be
answered at one place.*

*Answer should be brief and to-the-point and be supplemented
with neat sketches. Unnecessary long answer may result in
loss of marks.*

*Any missing or wrong data may be assumed suitably
giving proper justification.*

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Draw the self-bias circuit for an N-P-N transistor and estimate the Thevenin voltage, Thevenin resistance and input resistance overlooking the base node. 10
- (b) For the self-bias circuit above, find I_C , V_{CE} at Q-point provided that $\beta = 100$, load resistor = $2\text{ k}\Omega$, emitter resistor = $470\ \Omega$, $R_1 = 27\text{ k}\Omega$ and $R_2 = 4.7\text{ k}\Omega$, where $V_{BE} = 0.7\text{ V}$ and $V_{CC} = 10\text{ V}$. 10
2. (a) Design a single op-amp based logarithmic amplifier and exponential amplifier and give the input-output relation of each. 10

- (b) Define (i) virtual ground, (ii) CMRR, (iii) PSRR, (iv) slew rate, and (v) unity gain bandwidth for an op-amp. 5 × 2
3. (a) Design a class-B push-pull amplifier using BJT and calculate the maximum efficiency η . 10
- (b) Design a cascade current mirror using MOSFET and estimate the output impedance. 10
4. (a) Design an RC phase-shift oscillator for $f = 1$ kHz and calculate the values of the 3 R's in the phase shift loop, if $c = 0.1 \mu\text{F}$. 10
- (b) Identify the feedback type in the circuit as shown in Fig. 1 and calculate the gain with feedback A_{vf} . 10

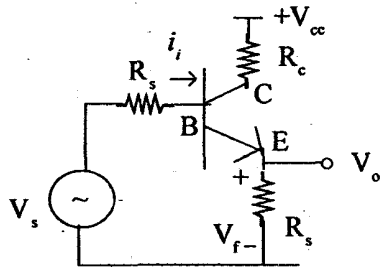


Fig. 1

Group B

5. (a) Design a full adder and give the Boolean expression of sum and carry-out. 10
- (b) Assuming 0 on the leftmost place, indicate positive and 9 on the leftmost place, indicate negative numbers using 10s complement addition for subtraction perform A-B, where (i) A = 045, B = 027; and (ii) A = 027, B = 045. 10

6. (a) Using Karnaugh map, do the minimization of the following functions : 5 + 5
- (i) $\sum m (0, 4, 8, 10, 11, 12, 13, 15)$
- (ii) $\prod M (0, 1, 4, 8, 9, 12, 15)$
- (b) Realize the Boolean expression $f = \bar{x}_1 + (\bar{x}_2 + \bar{x}_3) \cdot \bar{x}_4$ 10
7. (a) Design a 3-bit asynchronous up counter using 3XJK flip-flop and show the state. 10
- (b) Design an R-2R type DA converter and explain its operation. 10
8. Write short notes on the following : 2 × 10
- (a) Synchronous counter
- (b) Shift registers

Group C

9. Answer the following in brief : 10 × 2
- (i) Give the BCD equivalent of 58.
- (ii) Give the octal equivalent of 75 in decimal.
- (iii) Voltage-shunt negative feedback loop is needed in phase shift oscillator. (True/False)
- (iv) If $I_C = 200$ mA and $I_B = 1$ mA, what is the value of β ?
- (v) In saturation region, BE junction is — biased and BC junction is — biased.
- (vi) In a single op-amp non-inverting amplifier, if $R_f = 10$ k Ω and $R_s = 1$ k Ω , what is the output, if input = 1 mV ?

- (vii) If the open loop gain = A and feedback factor β , then D is given by _____.
- (viii) In cascade current mirrors, the dynamic range is reduced by _____.
- (ix) A/D flip flop can be realized by connecting an _____ after input J and feeding the output to input _____.
- (x) A transconductance amplifier will have a voltage signal at input and a _____ at its output.

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