W'08 : 7 AN : EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

Time : Three hours

Maximum Marks : 100

Answer FIVE *questions, taking* ANY TWO *from* **Group A**, ANY TWO *from* **Group B** *and* ALL *from* **Group C**.

All parts of a question (a, b, etc.) should be answered at one place.

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Group A

1. (*a*) Obtain an expression for the closed loop gain of a practical inverting op amp in terms of its circuit components. 6

(*b*) Derive an expression for the CMRR of an emitter-coupled differential amplifier. How can CMRR be changed ? 10

(*c*) Describe the principle of operation of an inverting, first order, low-pass filter using op amp and draw its frequency response curve. What are its advantages over a passive low-pass filter ? 4

2. (*a*) Calculate the ripple factor for an half-wave rectifier with a shunt capacitor filter and draw the time variation of load voltage. How does the ripple factor vary with load. 6

(*b*) What is SMPS ? Describe the principle of operation of a buck converter. 8

(*c*) A buck converter, having a switching frequency of 25 kHz, is to be operated with a duty cycle such that $0{\cdot}1 \leq D \leq 1$. The load is $R_L = 5\,\Omega$. Determine the value of critical inductance $L = L_C$ so that the current i_L is continuous. Here D is the buck converter voltage gain. 6

3. (*a*) Define slew rate of an op amp. How can you measure slew rate of an op amp. 5

(*b*) Explain the working of IC voltage regulator. What do you mean by percentage regulation ? 6

(*c*) Derive the expressions for outputs of integrator, multiplier and bridge amplifier using op amp. 9

4. (*a*) Derive the output voltage of an instrumentation amplifier using three non-inverting op amps in terms of gaining of individual stages. 8

(*b*) Describe the working of sample and hold circuit. 5

(*c*) Explain, with a block diagram, the universal balancing techniques for inverting and non-inverting op amps. 7

Group B

5. (*a*) What is the Barkhausen criterion for oscillation ? Draw the circuit of Wien bridge oscillator using op amp and derive its frequency of oscillation. 10

(*b*) Describe the principle of oscillation in a crystal oscillator. How can a clock be generated from it ? 4

(*c*) Explain, with a block diagram, the working of a function generator giving at least sine wave, square wave, and triangular wave outputs. 6

6. (*a*) Describe the working of a bistable multivibrator. How does it help in clock division ? 7

(*b*) Explain, with a block diagram, how FSK signal can be generated. What are BPSK and QPSK signals ? 8

(*c*) An FM transmitter has a frequency deviation of 20 kHz. Determine the percent modulation of this signal in the 88-108 MHz band when maximum permitted frequency deviation is 75 kHz. 5

7. (*a*) Calculate the beta cut-off frequency and the low-frequency value of alpha for a transistor amplifier having a gain bandwidth product of 1200 MHz and a low frequency beta of 90. 8

(*b*) What is PLL and how it can be used as FM demodulator ? 5

(*c*) Explain in detail the working of a balanced modulator. How does it differ from unbalanced AM. 7

8. (*a*) What is sequence generator ? 4

(*b*) Explain the working of a digital voltmeter. 7

(*c*) Describe, with a block diagram, the working of up-down synchronous counter with parallel carry. How can a counter be used for frequency measurement ? 9

Group C

9. Choose the *correct* answer for the following : 2 x 10

(*i*) The gain of common source FET amplifier, with mid-band gain A, at high frequency is

(*a*) A

(*b*) $\sqrt{2}A$

(*c*) $2\sqrt{2}A$

(*d*) $A/\sqrt{2}$.

(*ii*) By increasing the number of identical stages in an amplifier, the gain bandwidth product

(*a*) decreases

(*b*) becomes unity

(*c*) remains constant

(*d*) increases.

(*iii*) In three R-C combinations of a phase-shift oscillator, each R - C gives a phase shift of

(*a*) 60°

(*b*) 90°

(*c*) 30°

(*d*) 45°.

(*iv*) The maximum slew rate for output voltage, $V_0 = 2\sin\omega t$, of an op amp is

(*a*) ω

(*b*) 2ω

(*c*) $1/\omega$

(*d*) $2/\omega$.

(*v*) In op amp IC741, output taken from the pin number is

(*a*) 3

(*b*) 8

(*c*) 6

(*d*) 7

(*vi*) One of the drawbacks of FM signal is

(*a*) high noise

(*b*) limited range

(*c*) low signal strength

(*d*) None of the above.

(*vii*) The frequency of oscillation of a Hartley oscillator is

(*a*) $w = 1/LC$

(*b*) $w = 1/\sqrt{LC}$

(*c*) $w = 2\pi LC$

(*d*) $w = 2\pi/\sqrt{LC}$.

(*viii*) A resistive-ladder D/A converter does not require

(*a*) wide range of frequency

(*b*) wide range of bandwidth

(*c*) wide range of resistance values

(*d*) wide range of voltage.

(*ix*) In an amplifier, variation in β causes

(*a*) bias unstability

(*b*) bias stability

(*c*) zero bias

(*d*) None of the above.

(*x*) Thermal noise in transistor amplifier is also known as

(*a*) shot noise

(*b*) Schottky noise

(*c*) black noise

(*d*) Johnson noise.

S'09 : 7AN : EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

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Group A

1. (*a*) State the relative merits of FET op-amps and BJT op-amps. 3

(*b*) Design an op-amp differentiator that will differentiate an input signal with f_{max} = 100 Hz. 5

(*c*) Draw the simplified circuit diagram of an RF-IF amplifier IC and explain how this amplifier can be used as tuned as well as video amplifier. 6

(*d*) Draw a neat sketch showing an audio power amplifier using LM 380. Why is there no need to

(*Turn Over*)

use a separate heatsink ? Explain how the gain of the audio power amplifier can be increased by using positive feedback. 6

2. (*a*) Show that the ripple factor of the basic half-wave rectifier is 121 percent. 5

(*b*) The low frequency resistance of a power supply that consists of a full wave rectifier with a capacitor filter is to be less than 0·1 ohm. What is the minimum value of capacitance which can be used ? The power line frequency is 60 Hz. 8

(*c*) Why are electrolytic capacitors usually used in power supplies ? 3

(*d*) With reference to a power supply, what is bleeder resistance ? Why is it used ? 4

3. (*a*) Define input regulation and load regulation. 3

(*b*) What are the limitations of three terminal regulators ? 3

(*c*) Draw and explain the functional diagram of 723 regulator and explain how it provides short-circuit protection. How is current boosting achieved ? 8

(*d*) Using 7805, design a voltage regulator to get a voltage output of 7·5 V. It is given that the quiscent current I_Q is 4·2 mA for 7805. 6

4. (*a*) Sketch the transfer characteristics of an ideal comparator and a practical comparator. 3

(*b*) Draw and explain the circuit diagram of an inverting zero crossing detector. Sketch the output signal for a sinusoidal input. 5

(*c*) Using an op-amp, design an adder circuit to get the output V_0 as

$$(0{\cdot}1\ V_1 + V_2 + 10V_3)$$

where V_1, V_2 and V_3 are three inputs. Choose the feedback resistor, R_f, as 10 kΩ . 4

(*d*) Design a second-order Butterworth low-pass filter having a cut-off frequency of 1 kHz. The damping factor α is equal to 1·414. 8

Group B

5. (*a*) Draw the circuit diagram of Hartley oscillator and derive an expression for the frequency of oscillation. 6

(*b*) Describe various methods used to stabilise the amplitude of the output of an oscillator. 4

(*c*) Why does the frequency stability of a clapp oscillator increase as 9 m increases ? 3

(*d*) Using an op-amp, design a phase shift oscillator to oscillate at 100 Hz. 7

6. (*a*) Show, giving a mathematical proof, how a square law device can be used to generate an AM signal. 6

(*b*) A simple diode detector has a load of 500 kΩ in parallel with a capacitance of 100 pF. If the maximum modulation depth of the input signal is 80 percent, find the highest modulation frequency that can be detected without harmonic distortion. 4

(*c*) Derive an expression for the lock-in range of a PLL (phase locked loop). 7

(*d*) List out the important criteria governing the choice of IF (intermediate frequency) in a radio receiver. 3

7. (*a*) Determine the octal equivalent of the hexadecimal number AB.CD. 4

(*b*) Show that the width of a pulse generated by a monostable multivibrator is given by

$$T = 0{\cdot}69\ RC$$

where the symbols used have their usual meanings. 6

(*c*) Using op-amp 741, design a Schmitt trigger whose UTP = + 0·5 V and LTP = - 0·5V. 6

(*d*) Write down the truth table for a full subtractor. 4

8. (*a*) Using a neat block diagram, explain how a frequency counter can be used for measuring 'period'. 7

(*b*) The basic step of a 9 bit DAC is 10·3 mV. If 000000000 represents 0 V, determine the analog output for an input of 101101111. 3

(*c*) Draw the block diagram of a ramp type digital voltmeter and explain its working. 7

(*d*) Show that the NOR gate is a universal building block. 3

Group C

9. Answer the following in brief : 2 × 10

(*i*) Distinguish between linear ICs and digital ICs.

(*ii*) With reference to an op-amp, define PSRR.

(*iii*) With reference to a bleeder resistance in a power supply, why are carbon resistors preferable to wire wound resistors ?

(*iv*) Why are series regulators also called linear regulators ?

(*v*) State *five* important features of an instrumentation amplifier.

(*vi*) State the reasons for frequency stability of crystal oscillators.

(*vii*) What is the advantage that accrues when we use a RF amplifier in a superheterodyne receiver ?

(*viii*) In order to be used in a PLL, state *six* desirable features of a VCO.

(*ix*) With reference to an A/D converter, define 'resolution'.

(*x*) What is the minimum number of flip-flops needed to build a MOD-18 synchronous counter ?

W'09 : 7 AN : EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

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Group A

1. (*a*) Explain the difference between constant current bias and current mirror? 6

(*b*) With a neat sketch, analyse a typical op-amp equivalent circuit. What is the role of non-inverting terminal in op-amp? Why cannot feedback be given to this terminal for amplifier operation? 10

(*c*) A 10 V, 50 Hz sawtooth wave is superimposed on a 4 V sinusoidal signal. Find the maximum and

minimum pulsewidths when frequency of sawtooth is 10 times that of sine wave and ramp amplitude is 18 V. Assume a comparator reference of 2 V. 4

2. (*a*) A full-wave rectifier uses filter inductance $L = 20$ H and a load resistance $R_L = 20\,\text{k}\Omega$. A sinusoidal voltage $V = 300 \sin 2\pi \times 50\, t$ is applied to the input. Assuming the rectified output to contain second harmonic only, find (*i*) d.c. load current, (*ii*) d.c. output voltage, (*iii*) ripple factor, and (*iv*) ratio of this ripple to that without inductor filter. 8

(*b*) Explain the Q of LC filter. How can it be varied? 8

(*c*) Mention merits and demerits of π filtered full wave rectifier. 4

3. (*a*) Draw the functional diagram of CA 3085 voltage regulator and explain how current limiting and frequency compensation is achieved. 10

(*b*) Design a Zener diode of 6 V regulator for input fluctuations from 4 V to 8 V. 10

4. (*a*) The circuit (*Fig*.1) of the differential amplifier using ideal op-amp is shown :

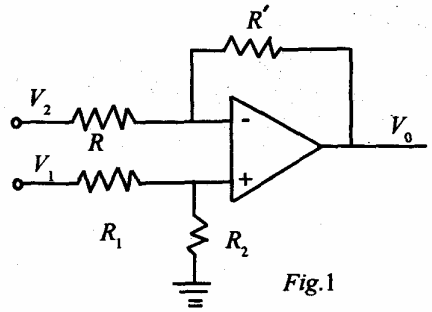

Fig.1

(*i*) Find the output voltage, V_0, and 2

(*ii*) Show that the output corresponding to common mode voltage $V_c = (V_1 + V_2)/2$ is zero, if $R'/R = R_2/R_1$. Find V_0 in this case. 4

(*iii*) Find CMRR of the amplifier, if $R'/R \neq R_2/R_1$. 2

(*b*) Find R_1 and R_f in the lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $w = 10{,}000$ rad/s. Use a capacitance of 0·01 μF. 8

(*c*) A 741 C op-amp is used as an inverting amplifier with a gain of 50. The voltage gain *vs*. frequency curve of 741 C is flat up to 20 kHz. What maximum peak-to-peak input signal can be applied without distorting the output. 4

Group B

5. (*a*) Assume the following values for the VCO circuit of $R_C = 1{\cdot}0\,\text{k}\Omega$, $R_E = 0{\cdot}1\,\text{k}\Omega$, $L = 10\,\mu\text{H}$, and $C = 100$ pF. Find the resonant frequency. 2

(*b*) A gain variation of + 10 % is expected for an amplifier with an internal gain of 100. How can this variation be reduced to + 1 %? 5

(*c*) Explain briefly about the conditions for maintaining oscillation in an oscillator. 8

(*d*) Draw the circuit diagram of crystal oscillator. Explain its operations. 5

6. (*a*) Design the bit error rate measuring instrument up to 10^{-5} error. Describe the synchronization technique used in the design. 10

(*b*) Design a clock synchronization circuit for noisy channel. 10

7. (*a*) Describe successive approximation technique for analog signals converted to digital signals. 8

(*b*) Show the external connections to 74181 to form a 4 bit subtractor. Label the input and output pins with binary states that occur when subtracting $13 - 7$ ($A = 13$, $B = 7$). 4

(*c*) Place the following values at the inputs of a 74181 : $A_3 - A_0 = 1001$, $B_3 - B_0 = 0011$ $S_3 - S_0 = 1101$ and $\bar{C}_N = 1$.

(*i*) With $M = 1$, determine the output $F(F_3 - F_0)$. 2

(*ii*) Change M to 0, and determine the output at $F(F_3 - F_0)$. 2

(*d*) Determine the decimal equivalent of the hexadecimal number $2A6_{16}$. 4

8. (*a*) Discuss briefly about digital frequency synthesizer circuits. 8

(*b*) Explain the generation of square waveform with the multivibrator circuit. How can the transients be reduced at edges of transitions ? 8

(*c*) What is a cascode amplifier ? What are its merits ? Why the cascode amplifier for video amplification needs specific figure of merits for IC used ? 4

Group C

9. Answer the following in brief : 2 x 10

(*i*) What is a window detector ?

(*ii*) With reference to op-amp, define CMRR.

(*iii*) Write the features of an instrumentation amplifier.

(*iv*) Draw a circuit for multiplication of two analog signals.

(*v*) What is race around problem in digital sequential circuit ?

(*vi*) How is an op-amp used as a sample and hold circuit.

(*vii*) What is a capture range and lock range of PLL ?

(*viii*) Design an amplifier with a gain of - 10 and input resistance equal to $10\,k\Omega$.

(*ix*) A full-wave rectifier uses an LC filter with $L = 20\,H$ and $C = 15\,\mu F$. The applied voltage is $V = 300 \sin 2\pi \times 50\,t$. Find the ripple factor.

(*x*) What is the difference between open loop and closed loop gain in op-amp ?

S'10 : 7 AN : EC 407 (1482)

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Group A

1. (*a*) Why is it that IC op amps invariably make use of level translator circuits ? 4

(*b*) Explain why high gain op amps generally possess limited bandwidth. 4

(*c*) Explain why many three-stage op amps have two feedback loops and one feed forward path. 4

(*d*) Using an op amp, design a second order low-pass filter with a cut-off frequency of 1 kHz. 8

2. (*a*) Give three reasons why an unregulated supply is inadequate for some applications. 4

(*b*) Define input regulation factor, output resistance and temperature coefficient for a voltage regulator. 5

(*c*) Explain why a switching regulator is capable of very high conversion efficiency. 3

(*d*) Can a three terminal fixed voltage regulator be used as a current source ? Using 7805, design such a circuit to supply a current of 1 A to a 10 ohm, 10 W load. 8

3. (*a*) Distinguish between positive and negative voltage regulators. 3

(*b*) Show that the secondary utilisation factor of a polyphase rectifier is given by

$$\sqrt{2/p} * \sin(\pi/p) / (\pi/p),$$

where p is the number of phases. Hence or otherwise, explain why p is selected to be 3. 8

(*c*) Show that an inductor input filter can achieve better regulation than the simple capacitor filter. 6

(*d*) For a bleeder resistance in a high voltage power supply, why are carbon resistors preferred over wire wound resistors ? 3

4. (*a*) Using three op amps, draw the circuit diagram of an instrumentation amplifier and derive an expression for the output voltage in terms of the input voltages and circuit resistances. 8

(*b*) Using an op amp, design an adder circuit whose output, V_0, is given by

$$V_0 = -(0 \cdot 1\ V_1 + V_2 + 10\ V_3)$$

where V_1, V_2 and V_3 are the inputs. 4

(*c*) Draw the circuit diagram of a saturation current and temperature compensated log amplifier. 4

(*d*) Explain how a basic comparator can be used as an inverting zero-crossing detector. Why is this circuit also called a sine wave to square wave generator ? 4

Group B

5. (*a*) What is the difference between a Sawtooth wave and a triangular wave ? 3

(*b*) The time period of an astable multivibrator using 555 timer is $T = 0 \cdot 693\ (R_A + 2\ R_B)\ C$. How will you modify the circuit so that duty cycle becomes 50 percent ? 3

(*c*) Draw the circuit diagram of an FET RC phase shift oscillator and derive an expression for the frequency of oscillation. 8

(*d*) Design a Wien bridge oscillator for $f_0 = 1$ kHz. 6

6. (*a*) For being used in a PLL (phase locked loop), describe the characteristics that a voltage controlled oscillator must possess

(*b*) A linear F/V converter is initially adjusted for $V_0 = 2{\cdot}8\,V$ at $F_{in\,(max)} = 10\,kHz$. Find the output voltage, if $F_{in} = 2{\cdot}5\,kHz$. 5

(*c*) Using IC 555, design a monostable multivibrator for a time delay T of 100 ms. 5

(*d*) Describe a suitable method to stabilise the amplitude of the output of an oscillator. 5

7. (*a*) Show mathematically how a square low device can be used to multiply a low frequency signal with high frequency signal. 5

(*b*) Describe the negative resistance characteristic of a tunnel diode. What is the use of the characteristic? 5

(*c*) Draw and explain the block diagram of an A/D converter. 5

(*d*) Explain a circuit that can be used as a frequency multiplier. 5

8. (*a*) Find the octal equivalent of the hexadecimal number $AB \cdot CD$. 4

(*b*) Draw the block diagram of a ramp-type digital voltmeter and explain its working. 7

(*c*) The basic step of a 9 bit D/A converter is 10·3 mV. If 000000000 represents 0 V, determine the output for an input of 101101111. 4

(*d*) Design a half adder using only NOR gates. 5

Group C

9. Choose the *correct* answer for the following : 1 x 20

(*i*) The heat generated by a μA 741 is 200 mW. Thermal resistance is 150° C/W and the ambient temperature is 25°C. The device temperature is

(*a*) 35°C

(*b*) 45°C

(*c*) 55°C

(*d*) 65°C

(*ii*) In a cascaded differential amplifier,

(*a*) RC coupling is used

(*b*) direct coupling is used

(*c*) a.c. coupling is used

(*d*) a.c. or d.c. coupling may be used.

(*iii*) Frequency doubling can be achieved by using

(*a*) log amplifier

(*b*) multiplier

(*c*) antilog amplifier

(*d*) adder.

(*iv*) The purpose of shielding wires in an active guard drive in instrumentation amplifiers is that

(*a*) it has fixed impedance as a transmission line

(*b*) it is used to match the impedance at two junctions

(*c*) it reduces differential mode noise pickup

(*d*) the balanced transmission ejects common mode noise component.

(*v*) An example of an isolation amplifier is

(*a*) 284J

(*b*) ICL 7600

(*c*) LM 335

(*d*) 74151.

(*vi*) The output voltage in a switching regulator for an input V_{in} and duty cycle δ is

(*a*) $V_{in}\,\delta$

(*b*) $V_{in}\,(1-\delta)$

(*c*) $V_{in}\,(1-\delta)/\delta$

(*d*) $V_{in}\,\delta/(1-\delta)$.

(*vii*) Back switching regulator means

(*a*) step up switching regulator

(*b*) step down switching regulator

(*c*) switching regulator with $V_0 = V_{in}$

(*d*) None of the above.

(*viii*) In BIFET op amps,

(*a*) negative supplies to be turned on before positive supplies are turned on

(*b*) positive supplies to be turned on before negative supplies are turned on

(*c*) both supplies can be turned on simultaneously

(*d*) the interval between the switching of positive and negative supplies should be 10 sec.

(*ix*) The LM 3911 temperature transducer generates - 10 mV/K. To achieve + 100 mV/K, one uses

(*a*) inverter with $R_2/R_1 = 9$

(*b*) non-inverter with $R_2/R_1 = 9$

(*c*) inverter with $R_2/R_1 = 10$

(*d*) non-inverter with $R_2/R_1 = 10$.

(*x*) To avoid false triggering in a comparator, we incorporate

(*a*) negative feedback

(*b*) hysteresis on positive feedback

(*c*) either positive or negative feedback

(*d*) triple modular redundancy.

(*xi*) ICL 8038 is capable of generating

(*a*) sine wave only

(*b*) square wave and triangular wave

(*c*) sine, square and triangular waves

(*d*) sine and triangualar waves.

(*xii*) A tone burst generator requires

(*a*) dual timer

(*b*) single timer

(*c*) single delayed timer

(*d*) VCO.

(*xiii*) The main advantage of MC 1422 timer over 555 timer is that

(*a*) it can produce large time delay

(*b*) no external components like resistor or capacitor required

(*c*) it offers completely independent variable threshold

(*d*) All of the above.

(*xiv*) In a SSB transmitter, one finds a

(*a*) class C audio amplifier

(*b*) tuned modulator

(*c*) class B RF amplifier

(*d*) class A RF output amplifier.

(*xv*) A PWM signal can be generated by

(*a*) one shot multivibrator

(*b*) astable multivibrator

(*c*) integrating a PPM signal

(*d*) differentiating a PPM signal.

(*xvi*) Which one of the following is inherently highly immune to noise?

(*a*) PAM

(*b*) PWM

(*c*) PPM

(*d*) PCM.

(*xvii*) A positive logic OR gate is the same as a negative logic

(*a*) NOR gate

(*b*) OR gate

(*c*) EX-OR gate

(*d*) AND gate.

(*xviii*) The minimum number of flip-flops needed to build a MOD-20 counter is

(*a*) 5

(*b*) 4

(*c*) 20

(*d*) 10.

(*xix*) When one input of an EX-OR gate is connected to logic 1, it functions as a

(*a*) NOT gate

(*b*) OR gate

(*c*) EX-OR gate

(*d*) NOR gate.

(*xx*) The quantisation error in an A/D converter or D/A converter is

(*a*) $\pm$ (1/2) LSB

(*b*) $\pm$ (1/2) V_{in}

(*c*) $\pm$ (1/2) V_{LSB}

(*d*) $\pm$ (1/2) V_0.

S'11 : 7 AN : EC 407 (1482)

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Group A

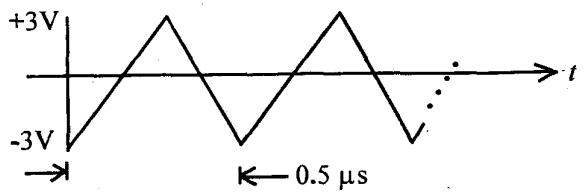
1. (*a*) List and explain the functions of all basic building blocks of an op-amp. 6

   (*b*) Describe six characteristics of an ideal op-amp. 6

   (*c*) State the advantages of FET op-amp over BJT op-amp. 4

   (*d*) The output of an op-amp voltage follower is a triangular wave as shown below for a square wave

input of frequency 2 MHz and 8 V peak-to-peak amplitude.



Determine the slew rate of the op-amp. 4

2. (*a*) Draw the circuit diagram of a full wave rectifier and show that its ripple factor = 0·482. 4

(*b*) A full wave rectifier is to supply 100 mA at 350 V with a ripple that must be less than 10 V. Specify the elements of a rectifier using a single L-section filter that will provide the desired results. 7

(*c*) With reference to a power supply, draw a short-circuit overload protection circuit and explain how it works. 6

(*d*) What is a swinging choke ? What is its advantage over a bleeder resistor ? 3

3. (*a*) Describe the characteristics of three terminal IC regulators. 4

(*b*) What are the voltage options available in 78 XX and 79 XX voltage regulators ? 4

(*c*) What is the principle of switch mode power supplies ? State their advantages and disadvantages. 6

(*d*) Design a voltage regulator using 723 to get a voltage output of 3 V. 6

4. (*a*) Using an op-amp, design an adder circuit whose output is 4

$$V_0 = -(0{\cdot}1\ V_1 + V_2 + 10\ V_3).$$

(*b*) Draw a sample and hold circuit. Explain its operation and indicate its uses. 6

(*c*) Explain why CMMR $\rightarrow \infty$ for an emitter-coupled differential amplifier when $R_E \rightarrow \infty$. 3

(*d*) Design a lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when ω = 10,000 rad/sec. Use a capacitance of 0·01 μF. 7

Group B

5. (*a*) State two conditions that must be satisfied for sustained oscillations. 3

(*b*) Draw the circuit diagram of a phase shift oscillator and derive an expression for the frequency of oscillation. 7

(*c*) Explain why crystal oscillators have a good frequency stability. 3

(*d*) Design a Wien bridge oscillator whose frequency of oscillation is 1 kHz. 7

6. (*a*) What is the difference between a sawtooth wave and a triangular wave ? Give circuits for respective one generation. 3

(*b*) Using 555, draw the circuit diagram of a monostable multivibrator and derive an expression for the time delay. 8

(*c*) Design a Schmitt trigger for UTP = + 0·5 V and LTP = - 0·5 V. 7

(*d*) State two advantages of CMOS Schmitt triggers. 2

7. (*a*) With reference to a PLL, define capture range, lock range and pull-in-time. 4

(*b*) Using a block diagram, explain how a PLL can be used as an AM demodulator. 5

(*c*) Describe the important criteria in the choice of IF for a radio receiver. 5

(*d*) A diode detector circuit with an efficiency of 90 percent represents an effective load of 250 kΩ across a source of modulated HF voltage. Determine the resistance and the capacitance to be used with the diode for satisfactory operation at modulation frequencies of 10 kHz and modulation depth of 80 percent. 6

8. (*a*) Determine the octal equivalent of the hexadecimal number DC.BA. 4

(*b*) Show that a NAND gate is a universal building block. 4

(*c*) Draw and explain the block diagram of a staircase ramp digital voltmeter. 8

(*d*) The basic step of a 9-bit DAC is 10·3 mV. If 000000000 represents zero V, determine the output voltage if the input is 101101111. 4

Group C

9. Choose the *correct* answer for the following : 10 x 2

(*i*) A non-inverting amplifier with a gain of 100 is nulled at 25°C. What will be the change in the output voltage, if the temperature rises to 50°C for an offset voltage drift of 0·15 mV/°C ?

(*a*) 3·75 mV

(*b*) 7·5 mV

(*c*) 375 mV

(*d*) 750 mV

(*ii*) A 741C op-amp is used as an inverting amplifier with a gain of 50. The voltage gain *vs*. frequency curve of 741C is flat up to 20 kHz. The maximum peak-to-peak input signal that can be applied without distorting the output is

(*a*) 3·98 V

(*b*) 7·96 V

(*c*) 159 mV

(*d*) 318 mV

(*iii*) In a half-wave rectifier, the peak value of the a.c. voltage across the secondary of the transformer is $20\sqrt{2}$ V. No filter is used. The maximum d.c. voltage across the load will be

(*a*) 28·28 V

(*b*) 14·14 V

(*c*) 20 V

(*d*) 9 V

(*iv*) The function of a bleeder resistor in a power supply is

(*a*) same as that of load resistor.

(*b*) to ensure a minimum current drain in the circuit.

(*c*) to increase the output d.c. voltage.

(*d*) to increase the output current.

(*v*) An example of a log/anti-log amplifier IC chip is

(*a*) AD 533

(*b*) AD 534

(*c*) 755

(*d*) LF 398

(*vi*) In a bistable multivibrator, commutating capacitor is used

(*a*) to increase the base storage charge.

(*b*) to provide a.c. coupling.

(*c*) to increase the speed of response.

(*d*) for all of the above.

(*vii*) An oscillator of the LC-type that has a split capacitor in the tank circuit is

(*a*) Hartley oscillator.

(*b*) Colpitts oscillator.

(*c*) Wein bridge oscillator.

(*d*) negative resistance oscillator.

(*viii*) An astable multivibrator can be used as

(*a*) squaring circuit.

(*b*) comparator.

(*c*) frequency-to-voltage converter.

(*d*) voltage-to-frequency converter.

(*ix*) One of the advantages of base modulation over collector modulation of a transistor class C amplifier is

(*a*) lower modulating power required.

(*b*) higher power output per transistor.

(*c*) better efficiency.

(*d*) better transmission.

(*x*) In order to build a MOD-18 counter, the minimum number of flip-flops needed is

(*a*) 18

(*b*) 9

(*c*) 5

(*d*) 4

S'12:7AN:EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

Time : Three hours

Maximum Marks : 100

Answer FIVE *questions, taking* ANY TWO *from* **Group A,** ANY TWO *from* **Group B** *and* ALL *from* **Group C.**

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Figures on the right-hand side margin indicate full marks.

Group A

1. (*a*) For the amplifier circuit, shown in Fig. 1, $R_1 = 10\ k\Omega$, $R_f = 100\ k\Omega$, $V_i = 1$ V. A load of 25 kΩ is connected to the output terminal. Calculate (*i*) i_1, (*ii*) V_0, (*iii*) I_L and total current i_0 into the output pin. 8

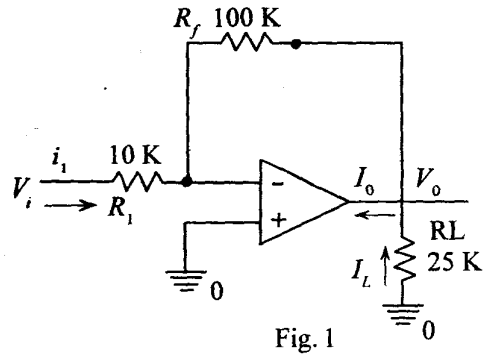

Fig. 1

(Turn Over)

(*b*) What are the characteristics of ideal operational amplifier? 3

(*c*) Explain how constant current source circuit improves the CMRR of the op amp. 9

2. (*a*) Explain the operation of full-wave rectifier with a neat diagram and obtain the expression for rectifier efficiency η. 10

(*b*) A half-wave rectifier is used to supply 24 V d.c. to a resistive load of 500 Ω and the diode has a forward resistance of 50 Ω. Calculate the maximum value of the a.c. voltage required at the input. 6

(*c*) What is meant by peak inverse voltage in rectifiers? 2

(*d*) What is regulated power supply? 2

3. (*a*) Explain about the operation of series op amp regulator with a neat block diagram. 8

(*b*) Describe the characteristics of IC voltage regulators. 4

(*c*) In Fig. 2, let $V_{EB(ON)} = 1$ V, $\beta = 15$, $V_L = 5$V. Calculate the output current coming from 7805 and I_C coming from transistor Q_1 for loads 100 Ω and 5 Ω. 8

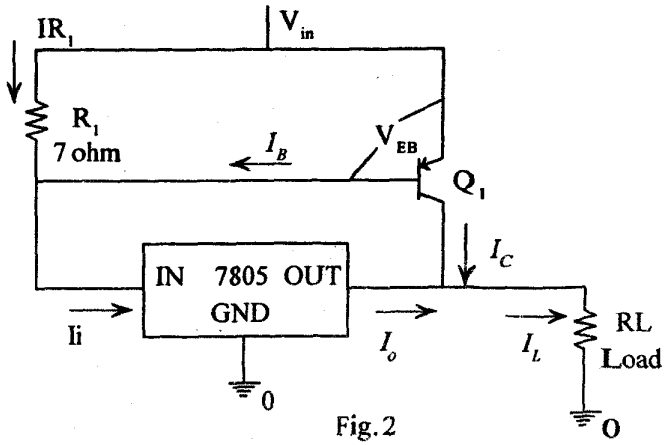

Fig. 2

4. (*a*) Draw the circuit diagram of logarithmic amplifier and explain its operation. 8

(*b*) Draw the output waveform for a square wave of 1V peak at 100 Hz applied to the differentiator. 2

(*c*) Design a wide band pass filter having $f_L = 400$ Hz, $f_H = 2$ kHz and pass band gain of 4. Find the value of Q for the filter? 6

(*d*) Briefly explain about the applications of comparator. 4

Group B

5. (*a*) Explain the operation of non-stable multivibrator using op amp, and derive the expression for ON and OFF state time periods. 12

(*b*) In a voltage controlled oscillator, applied control voltage is 3 V, timing resistor, $R_t = 5$ k Ω, timing capacitor $C_t = 10$ μF. Find the frequency of oscillation. 3

(*c*) Determine the value of R_f necessary for the circuit shown in Fig. 3 to operate as an oscillator and find the frequency of oscillation. 5

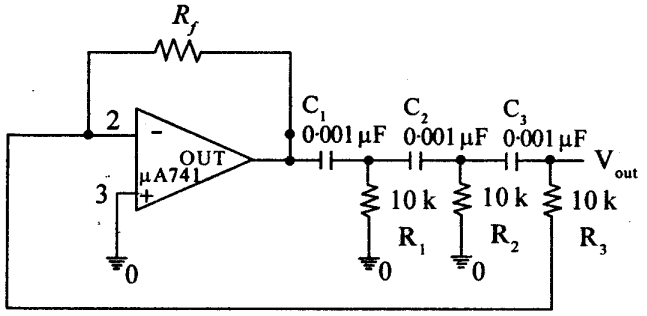

Fig. 3

6. (*a*) Explain how PLL can be used in frequency multiplier and AM detector circuits. 10

(*b*) With reference to a PLL, define capture range, lock range, and pull-in-time. 3 × 2

(*c*) Derive an expression for the output voltage in inverting summer. 4

7. (*a*) Calculate the values of LSB, MSB and full-scale output for an 8 bit DAC, if the applied input is in the range of 0 to 10 V range. 4

(*b*) Explain the operation of successive approximation analog-to-digital converter with a neat diagram. 12

(*c*) Define the parameter resolution and settling time of digital-to-analog converter. Obtain the value of resolution for an 8 bit DAC. 4

8. (*a*) In a digital voltmeter, a reference voltage of 2 V is used, if both $3\frac{1}{2}$ and $4\frac{1}{2}$ digit DVM are used. Calculate the resolution of DVM in both the cases and show which one gives better resolution ? 6

(*b*) Draw the circuit diagram of non-inverting integrator and explain in detail about its frequency response characteristics. 10

(*c*) Briefly explain the operation of sample-and-hold circuit. 4

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) A non-stable multivibrator has

(*a*) both the states as stable states.

(*b*) makes transition from one state to another when the trigger applied.

(*c*) both the states as unstable states.

(*d*) one stable state and one quasi-stable state.

(*ii*) IC LF 198 is an example of

(*a*) sample-and-hold circuit.

(*b*) log amplifier.

(*c*) antilog amplifier.

(*d*) voltage-to-frequency converter.

(*iii*) A non-inverting amplifier has input resistance $R_1 = 100\ \Omega$ and feedback resistance $R_f = 10\ k\Omega$. Its gain value is

(*a*) 10

(*b*) 101

(*c*) - 100

(*d*) - 200

(*iv*) The important feature of instrumentation amplifier is

(*a*) low CMRR.

(*b*) high output impedance.

(*c*) high gain stability.

(*d*) high d.c. offset.

(*v*) The output produced by ideal differentiator is

(*a*) $V_0 = -R_f C_1 \, dV_i/dt$

(*b*) $V_0 = (-1/R_f C_1)\,(dV_i/dt)$

(*c*) $V_0 = (-R_f C_1)\,(dI_i/dt)$

(*d*) $V_0 = (-1/R_f C_1)\,(dI_i/dt)$

(*vi*) The other name of one shot vibrator is

(*a*) Schmit trigger.

(*b*) monostable multivibrator.

(*c*) bistable multivibrator.

(*d*) astable multivibrator.

(*vii*) Which one of the following is true for narrow band pass filter ?

(*a*) $Q < 10$

(*b*) $Q > 10$

(*c*) $Q < 5$

(*d*) $Q = 1$

(*viii*) The time period of IC 555 monostable multivibrator operation is

(*a*) 1·38 RC

(*b*) 1·1 RC

(*c*) 1·45 RC

(*d*) 13·8 RC

(*ix*) The number of frequencies produced at the output of binary FSK modulator is

(*a*) two.

(*b*) infinite.

(*c*) power of two.

(*d*) three.

(*x*) The basic step of 4 bit DAC is 10 mV. If 0000 represents 0 V, what is the output produced, if the input is 1011 ?

(*a*) 110 mV

(*b*) 11 mV

(*c*) 110 mV

(*d*) 1·1 mV

W'12: 7AN: EC407(1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

Time : Three hours

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Group A

1. (*a*) Why is it that BIFET operational amplifiers have extremely low input bias current levels ? 3

(*b*) Describe two methods of offset nulling that might be used with a 741 op amp. 5

(*c*) Sketch the circuit of an op amp difference amplifier and derive an expression for the output in terms of the input. 6

(*d*) Design a capacitor-coupled voltage follower using a 741 op amp. The lower cut-off frequency of the circuit is 70 Hz and load = 4 kΩ. 6

2. (*a*) Distinguish between a dual and a dual tracking regulated power supply. 4

(*b*) Why is it desirable for a power supply to have a low output impedance ? 3

(*c*) What is the purpose of a bleeder resistance ? With reference to a bleeder resistance, why are carbon resistors preferable to wire wound resistors ? 5

(*d*) A half wave rectifier output is smoothed by a capacitor C and 20 V is fed to a load of 500 ohm. Maximum ripple amplitude is 10 per cent of the average output voltage. The input frequency is 60 Hz. Determine the value of C. 8

3. (*a*) Draw the circuit diagram of a simple Zener diode voltage regulator and explain how the circuit operates. 4

(*b*) Sketch a foldback current limiting circuit for a voltage regulator and explain the operation of the circuit. 5

(*c*) How can current boost be obtained in a three terminal regulator ? 14

(*d*) Using LM 217, design a IC voltage regulator to provide a 6 V fixed output. The supply voltage is 15 V. 7

4. (*a*) List the basic differences between Norton's amplifier and conventional op amp. 4

(*b*) Explain how a multiplier can be built using log amplifiers. 4

(*c*) Draw the circuit diagram of a dual op amp instrumentation amplifier. What is its drawback when it is compared with the triple op amp instrumentation amplifier ? 4

(*d*) Design a Sallen-Key unity gain low pass active filter to meet the following requirements : (*i*) Roll of rate = −40 dB/decade, (*ii*) pass band as flat as possible, (*iii*) cut-off frequency = 2 kHz, and (*iv*) gain at DC = 5. 8

Group B

5. (*a*) Draw the circuit diagram of a Hartley oscillator and derive an expression for the frequency of oscillation. 5

(*b*) Describe procedures for stabilising the amplitude of the output of an oscillator. 6

(*c*) Why does the frequency stability of a clapp oscillator increase as g_m increases ? 3

(*d*) Design a Wein bridge oscillator whose frequency of oscillation f_0 is 625 Hz. 6

6. (*a*) Explain how a monostable multivibrator can be used to detect a missing pulse. 5

(*b*) Explain how a triangular wave can be converted into a sine wave. 5

(*c*) State the important features of grounded capacitor voltage-controlled oscillators and emitter-coupled voltage-controlled oscillators. 3

(*d*) Using a 555 timer, design an astable multivibrator. Given : frequency $f_0 = 50$ kHz and duty cycle $D = 75$ per cent. 7

7. (*a*) Show that, for tone modulated AM, the maximum efficiency is 33 per cent. 4

(*b*) Explain how a DSB-SC signal can be demodulated by carrier re-insertion and envelope detection. 6

(*c*) Using a neat block diagram, explain how a PLL can be used as a FSK demodulator. 5

(*d*) Select filter components for a PLL whose lowest frequency from the phase detector is 5 Hz. A 0·5 percent variation in frequency is allowable. 5

8. (*a*) Convert the base 3 number 1021121·121 directly into a base 9 number. Do not convert to base 10 number. 3

(*b*) Draw and explain the block diagram of a ramp-type digital voltmeter. 7

(*c*) Show that the NOR gate is a universal building block. 4

(*d*) Using a neat sketch, explain the working of a parallel comparator (flash) analog-to-digital converter. 6

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) In a cascaded differential amplifier,

(*a*) RC coupling is used.
(*b*) direct coupling is used.
(*c*) AC coupling is used.
(*d*) AC or DC coupling may be used.

(*ii*) How many op amps does a window comparator require ?

(*a*) 1
(*b*) 2
(*c*) 3
(*d*) 4

(*iii*) A multiplier, which can accept input voltage of any polarity and can produce output voltages of any polarity, is called

(*a*) universal multiplier.
(*b*) one quadrant multiplier.
(*c*) two quadrant multiplier.
(*d*) four quadrant multiplier.

(*iv*) Thermal shutdown in 78 XX will occur at

(*a*) 70 °C
(*b*) 90 °C
(*c*) 110 °C
(*d*) 135 °C

(*v*) The output voltage of a switching regulator for an input V_{in} and duty cycle δ is given by

(*a*) $V_{in}\,\delta$
(*b*) $V_{in}(1-\delta)$
(*c*) $V_{in}(1-\delta)/\delta$
(*d*) $V_{in}\,\delta/(1-\delta)$

(*vi*) Which one of the following is not a dual timer ?

(*a*) NE 556
(*b*) MC 3456
(*c*) MC 1422
(*d*) XR 2556

(*vii*) In order to use PLL in a frequency synthesizer, one additionally requires

(*a*) frequency counter.
(*b*) oscillator
(*c*) analog multiplier.
(*d*) high pass filter.

(*viii*) Second order filters, in which the damping factor exceeds 0·7, are called

(*a*) Butterworth filters.

(*b*) Chebyshev filters.
(*c*) Bessel filters.
(*d*) Sallen-Key filters.

(*ix*) Quantisation error in ADC or DAC is

(*a*) $\pm$ (1/2) LSB
(*b*) $\pm$ (1/2) V_{in}
(*c*) $\pm$ (1/2) V_{LSB}
(*d*) $\pm$ (1/2) V_0

(*x*) A positive logic AND gate is same as a

(*a*) negative logic AND gate.
(*b*) negative logic NAND gate.
(*c*) negative logic NOR gate.
(*d*) negative logic OR gate.

W'13: 7AN: EC407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

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Group A

1. (*a*) Explain, with help of circuit diagrams, the followings which are related to op-amp : (*i*) Virtual ground, (*ii*) CMRR, (*iii*) PSRR, (*iv*) input bias current. 4 × 2

   (*b*) Draw an inverting op-amp integrator circuit and its equivalent circuit. Find the expression for output voltage of the non-inverting integrator. 7

   (*c*) Describe universal offset voltage balancing technique for an op-amp. 5

2. (*a*) Explain the working principle of a regulated power supply using Zener diode over the range of input voltage variation V_{min} to V_{max}. 7

(*b*) Draw a full-wave rectifier with a capacitor filter and derive the expression for ripple power. 8

(*c*) Explain the principle of UPS operation. 5

3. (*a*) Draw the circuit of a half-wave rectifier using IC 741 op-amp with positive input and find the expression for output voltage. 10

(*b*) Explain the working principle of a feedback limiter circuit. 4

(*c*) What is short circuit protected regulator and dual tracking regulator ? 6

4. (*a*) Difference mode gain of a DIFF AMP is $A_d = 2000$. Calculate the output voltages for (*i*) CMRR = 100, and (*ii*) CMRR = 10,000, if the inputs are $V_1 = +1{\cdot}0$ mV and $V_2 = +0{\cdot}9$ mV and show the effect of high CMRR. Assume V_i applied at 1 mV input. 5

(*b*) Find the expression for overall output voltage of a differential amplifier with three op-amps. 8

(*c*) Find the expression for output voltage of a logarithmic amplifier and design a two input multiplier. 4

(*d*) Draw the zero-crossing detector ? Explain its function. 3

Group B

5. (*a*) Draw the circuit diagram of a RC-phase shift oscillator using op-amp and obtain the frequency of oscillation. 12

(*b*) Describe the working principle of a function generator that gives square wave and triangular wave of same frequency. 4

(*c*) What is VCO ? How does it get represented, say f_c, in transfer function form ? 4

6. (*a*) What is a square law detector ? Explain with a block diagram. How does it work for a selected range of frequencies ? 7

(*b*) What is a DSB-SC system ? Explain how, using balanced modulator, DSB-SC signal can be generated. How does it differ in shape from 100 % AM ? 8

(*c*) What is synchronous detection ? How is synchronous detection affected by phase error and frequency error ? How can you obtain coherent carrier at receiver for this circuit ? 5

7. (*a*) Describe the principle of working of a R-2R digital-to-analog converter. What is the minimum and maximum values of gain for it ? How can a digital-to-analog converter be used as current-to-voltage converter ? 10

(*b*) Draw the block diagram of an astable multivibrator using op-amps and explain its working principle. 5

(*c*) What is a digital frequency synthesizer ? How can a desired frequency be obtained from it ? 5

8. Write notes on the following : 8 + 6 + 6

(*a*) Video amplifier

(*b*) Digital voltmeter

(*c*) Frequency multiplier.

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) Output of an inverting op-amp is 10 sin *wt*. Slew rate of the amplifier is

(*a*) W
(*b*) 10
(*c*) $10\,W$
(*d*) $10 \cos wt$.

(*ii*) The range of time, within which a degree of certainty can be determined between a true value and an estimated value of communicating signals, is known as

(*a*) confidence interval.
(*b*) delay interval.
(*c*) hopping time.
(*d*) spreading time.

(*iii*) GMSK is a special care of

(*a*) QAM
(*b*) FSK
(*c*) QPSK
(*d*) PSK

(*iv*) The circuit used to convert FM signal into its corresponding AM siganl, with the help of a frequency dependent circuit, is known as

(*a*) encoder.
(*b*) decoder.
(*c*) frequency discriminator.
(*d*) slope detector.

(*v*) If input resistance is infinite and feedback resistance is zero, then a non-inverting op-amp acts as a

(*a*) integrator.
(*b*) differential amplifier.
(*c*) inverting op-amp.
(*d*) voltage follower.

(*vi*) In a ROM memory of sixteen 8-bit words, 16 memory elements are arranged in a 4×4 array. This topology is called

(*a*) coincident selection.
(*b*) matrix selection.
(*c*) linear selection.
(*d*) parallel selection.

(*vii*) An AM transmitter has carrier power output of 50 W. Total power produced with 80% modulation is

(*a*) 66 W
(*b*) 60 W
(*c*) 40 W
(*d*) 86 W

(*viii*) For a filter, when the transition band between passband and stopband is very narrow, it is known as

(*a*) soft roll-off.
(*b*) hard roll-off.
(*c*) slow roll-off.
(*d*) fast roll-off.

(*ix*) The sampler, which uses sampling and hold circuit, is called

(*a*) flat top sampling.
(*b*) natural sampling.
(*c*) ideal sampling.
(*d*) switching sampling.

(*x*) If two different cascaded tuned amplifier circuits are tuned to slightly different frequencies to obtain increased bandwidth with a flat passband and steep sides, the technique is known as

(*a*) double-tuned.
(*b*) flat-tuned.
(*c*) stagger-tuned.
(*d*) frequency-tuned.

S'14:7AN:EC407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

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Group A

1. (*a*) Using an op amp, explain how you will build a negative resistance converter. Derive an expression for the negative resistance that is simulated. **8**

(*b*) Using a T-network and an op amp, draw the circuit diagram of a high sensitivity I - V converter. Explain the need for JFET input and MOSFET input op amps in a high sensitivity I - V converter. **6**

(*c*) Describe offset nulling for a LM 311 voltage comparator using a neat sketch. **6**

2. (*a*) Draw the circuit diagram of a precision half wave rectifier and explain how it works. **6**

(*b*) A 10 V precision voltage reference has a maximum thermal coefficient of 1 ppm/°C. Find the variation in output voltage when the temperature changes from 0°C to 70°C. 4

(*c*) With reference to a regulator, describe short-circuit protection and current fold-back protection. 7

(*d*) How does a switching regulator achieve higher efficiency ? 3

3. (*a*) Draw the schematic diagram of an analog multiplier using logarithmic amplifier made of op amps. 10

(*b*) Design a two input amplifier with CMRR = 500 using op-amp with ideal characteristics. 10

4. (*a*) Explain how ground loop interference can be eliminated using a difference amplifier. 4

(*b*) State the relative merits of triple op amp instrumentation amplifiers and dual op amp instrumentation amplifiers. 4

(*c*) Design a low pass first order active filter to meet the following specifications : (*i*) - 3 dB frequency of 1 kHz, (*ii*) d.c. gain = 20 dB and (*iii*) input resistance ≥ 10 k Ω. 3 × 4

Group B

5. (*a*) Draw the circuit diagram of an op amp based Wien bridge oscillator and derive an expression for the frequency of oscillation. 7

(*b*) Explain how a limiter can be used to stabilise amplitude in a Wien bridge oscillator. 4

(*c*) Using 555 timer, design a free running multivibrator for a frequency f_0 = 50 kHz and duty cycle D = 75 percent. 6

(*d*) State the advantages of emitter-coupled voltage controlled oscillator. 3

6. (*a*) Draw and explain the circuit diagram of a CMOS crystal oscillator. Why does it have high degree of frequency stability ? 8

(*b*) Using neat sketches, describe (*i*) triangular to sine wave converter and (*ii*) sine wave to triangular wave converter. 6

(*c*) Design a ICL 8038 waveform generator for a frequency f_0 = 10 kHz. Assume V_{cc} = 15 V. 6

7. (*a*) What is the need for pre-emphasis ? Explain the working of pre-emphasis and de-emphasis circuits in public address system. 7

(*b*) A carrier signal of 600 V RMS is applied to a 75 ohm antenna. What is the carrier power ? Determine the total sideband power and total radiated power at 75 percent amplitude modulation. 5

(*c*) Using neat sketches, explain how the *p-n* junction can be used to design voltage to frequency converter ? 4

(*d*) State and prove Nyquist's sampling theorem. 4

8. (*a*) Using a neat sketch, describe the working of a weighted capacitor D/A converter. 8

(*b*) What are the two reasons on account of which $\Sigma - \Delta$ A/D converters use feedback ? 4

(*c*) Show that a positive logic AND gate is the same as a negative logic OR gate. 4

(*d*) Write the truth tables for half subtractor and full subtractor. 4

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) A 741 inverting amplifier with a gain of –2 is driven by a ± 10 V peak-to-peak triangular wave as shown in Fig. 1:

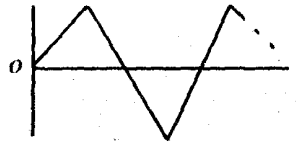
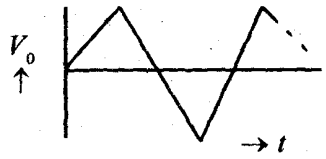


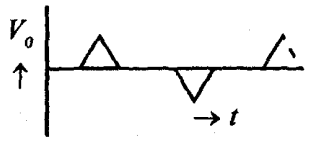
Fig. 1

The waveform at the output will be

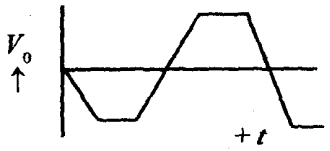
(*a*)



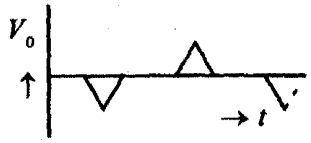
(*b*)



(*c*)



(*d*)



(*ii*) CMRR in dB is given by

(*a*) $10 \log_{10}(A_{dm}/A_{cm})$

(*b*) $10 \log_{2}(A_{dm}/A_{cm})$

(*c*) $10 \log_{e}(A_{dm}/A_{cm})$

(*d*) $20 \log_{10}(A_{dm}/A_{cm})$

(*iii*) KRC filters are also called

(*a*) passive filters,

(*b*) notch filters.

(*c*) all pass filters.

(*d*) Sallen key filters.

(*iv*) For a track and hold amplifier, the feed through rejection ratio = 80 dB. The hold mode voltage changes by 10 V. The change in output voltage equals

(*a*) 1 mV

(*b*) 2 mV

(*c*) 10 mV

(*d*) 20 mV

(*v*) For a quadrature oscillator, the frequency of oscillator is given by

(*a*) 2 ΠRC

(*b*) 1/(2 ΠRC)

(*c*) $1/(\sqrt{6}\ \Pi RC)$

(*d*) 1/(ΠRC)

(*vi*) The output voltage of a regulator changes by 3 mV when the input is varied from 7 V to 25 V. Its line regulation is equal to

(*a*) 0·17 mV/V

(*b*) 6 V/mV

(*c*) 54 mV/V

(*d*) 18·003 mV/V

(*vii*) Consider a DAC based A/D converter. To convert a full scale input, a 12 bit ADC with a 1 MHz counter clock will need

(*a*) 4·096 ns

(*b*) 4·096 μs

(*c*) 4·095 ms

(*d*) 40·95 ms

(*viii*) The maximum carrier frequency change for FM broadcast radio is given to be ± 75 kHz. An FM broadcast carrier is deviated by ± 30 kHz. The percentage of modulation is

(*a*) 25

(*b*) 40

(*c*) 30

(*d*) 75

(*ix*) The maximum VCO frequency of CMOS PLLs is typically of the order of

(*a*) 10 kHz

(*b*) 100 kHz

(*c*) 10 MHz

(*d*) 20 MHz

(*x*) The outputs of two 2-input NOR gates are cross-coupled. The result is a

(*a*) D flip-flop

(*b*) T flip-flop

(*c*) JK flip-flop

(*d*) SR flip-flop