

PULSE AND DIGITAL CIRCUITS*Time : Three hours**Maximum marks : 100*

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

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answered at one place.*

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Group A

1. (a) Show that $(x + y)(x' + y') = xy' + x'y + y$ by using
de Morgan's laws. 6
- (b) Find the complement of the following two functions : 4
 $f_1 = x'yz' + x'y'z$ and $f_2 = x(y'z' + yz)$
- (c) Express the Boolean function $f = xy + x'z$ in a
product of maxterm form. 6
- (d) Define positive and negative logic with an example
of each. 4

2. (a) Simplify the Boolean function
 $f = \Sigma m (0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$
 Implement the simplified function using NAND gates. 12
- (b) Realize AND logic by using only Exclusive-OR logic gates. 4
- (c) Define essential prime implicant, maxterm and minterm. 4
3. (a) Reduce the following function using Karnaugh map and implement with NAND gates only: 10

$$f = \Sigma m (1, 2, 4, 5, 7, 9, 10, 11, 13, 14).$$

- (b) Realize a minimised PLA design of the following switching functions: 10

$$f_1(x_1, x_2, x_3, x_4) = \Sigma (2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$$

$$f_2(x_1, x_2, x_3, x_4) = \Sigma (2, 3, 5, 6, 7, 10, 11, 14, 15)$$

$$f_3(x_1, x_2, x_3, x_4) = \Sigma (6, 7, 8, 9, 13, 14, 15)$$

4. (a) Convert $(359.23)_{10}$ into binary. 8
- (b) Evaluate in hexadecimal the following expression: 10
- $$(3569)_{10} + (12956)_8$$
- (c) Realize a 4-bit full binary adder with the help of half address. 2

Group B

5. (a) Explain the working of a master-slave JK flip-flop. Describe the advantage over single stage JK flip-flop. 10
- (b) Write down the truth table of D and T flip-flops with respective clocks. 4
- (c) Convert a SR flip-flop into a JK flip-flop. 6

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(Continued)

6. (a) Design a sequence detector that detects the sequence 0101 in a given binary sequence. Assume that the detector can detect overlapping sequences. 10
- (b) Describe functions of a monostable multivibrator. 10
7. (a) Design synchronous decade counter. 10
- (b) How can decade counter be used as divide by 5 counter? 10
8. Write short notes on *any two* of the following: 2×10
- (i) Schmidt trigger
- (ii) Astable multivibrator
- (iii) Fault detection in sequential circuits.

Group C

9. Choose the *correct* answer for the following: 2×10
- (i) $A \oplus 1$ is equal to
- (a) \bar{A}
- (b) A
- (c) 1
- (d) 0
- (ii) $A \cdot (A + B)$ is equal to
- (a) A
- (b) B
- (c) \bar{A}
- (d) \bar{B}

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(Turn Over)

(iii) $(32)_{10} = (\text{---})_2$

(a) 111111

(b) 100000

(c) 100001

(d) 100100

(iv) The standard form of $f(A, B, C) = A + B + C$ is

(a) $ABC + B\bar{C}A$

(b) $ABC + BC\bar{A} + \bar{B}CA$

(c) $\bar{A}\bar{B}\bar{C} + ABC$

(d) $ABC + A\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$
 $+ \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$

(v) In PLA

(a) AND array alone is programmable.

(b) OR array alone is programmable.

(c) both AND and OR are programmable.

(d) both AND and OR are not programmable.

(vi) If $J = K$ in a JK flip-flop,

(a) $Q_{n+1} = \bar{Q}_n$

(b) $Q_{n+1} = Q_n$

(c) $Q_{n+1} = 1$

(d) $Q_{n+1} = 0$

(vii) If $S = 0, R = 1$ in a SR flip-flop,

(a) $Q_{n+1} = \bar{Q}_n$

(b) $Q_{n+1} = Q_n$

(c) $Q_{n+1} = 0$

(d) $Q_{n+1} = 1$

(viii) If $f(x)$ is independent of x_i ,

(a) $df(x)/dx_i = 0$

(b) $df(x)/dx_i = 1$

(c) $df(x)/dx_i = x_i$

(d) $df(x)/dx_i = \bar{x}_i$

(ix) The minimum number of select signals necessary for a 4 to 1 multiplexer is

(a) 4

(b) 1

(c) 2

(d) 5

(x) Minimum number of flip-flops necessary to design a mod-10 counter is

(a) 10

(b) 4

(c) 2

(d) 5

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Group A

1. (a) State the distributive laws and explain the duality principle. 6
- (b) Prove the following: 6

$$\overline{(AB + BC + CA)} = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}.$$
- (c) Draw the block diagram of programmable logic array (PLA) and explain how it can be used to implement logic functions with an example. 8
2. (a) Realize EXCLUSIVE-OR logic function using only NAND gates. 6
- (b) Minimize the logic function using K-map and show the logic gate realization of the function 10

$$f = \sum_m \{1, 5, 6, 7, 11, 12, 13, 15\}.$$
- (c) Implement the AND logic function $Y = AB$ using a 2:1 multiplexer. 4

3. (a) Explain the Quine-McCluskey method of simplifying logic function using the five variable logic expression.
 $f = ABD + ACE + BCDE + ADE + ABDE + BCDE$. 12
 (b) State and explain the de Morgan's theorem. 3
 (c) Given the logic expression $y = (x_1x_2 + x_3x_4)$, find the Boolean difference with respect to x_3 . 5
4. (a) Write the corresponding minterm and maxterm for the following, using minimum number of variables:
 (i) m_8 , (ii) m_{44} , (iii) M_{51} , (iv) M_{18} . 4
 (b) Discuss about (i) fault classes, and (ii) fault models. 6
 (c) Give the truth table for full adder and write the logic expressions for sums (S) and carry (C_y). Also, draw the logic gate realization for sum and carry out using only NOR gates. 10

Group B

5. (a) Distinguish between synchronous and asynchronous counter circuits. Also, state the disadvantages of asynchronous counter circuit compared to synchronous counter circuit. 6
 (b) Minimize the state table of the FSM using partitioning procedure: 14

Present State	Next State		Output
	$w=0$	$w=1$	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

6. (a) Draw the excitation table for J-K flip-flop. 3
 (b) Design a asynchronous sequential circuit that has an input w an output z , such that when pulses are applied to w , the output z is equal to 0, if the number of previously applied pulses is even and $z = 1$ if the number of pulses is odd. Assume that w takes the values 0 or 1 depending on whether there is no pulse or a pulse at the input at any cycle. 17
7. (a) Explain how J-K flip-flop can be operated as (i) D flip-flop, and (ii) T flip-flop. 4
 (b) What is meant by pulse mode circuit? Discuss the basic model of this circuit. 10
 (c) Draw the circuit diagram of 3-bit ripple counter and explain its operation using a timing diagram. 6
8. Write short notes on the following: 10 × 2
 (a) Finite state recognisers and deterministic recognisers
 (b) State assignment in asynchronous sequential circuits.

Group C

9. Write the correct answer for the following: 2 × 10
 (i) The dual of $A - B + C$ is
 (a) $A \cdot B \cdot C$
 (b) $(\bar{A} + \bar{B}) + \bar{C}$
 (c) $(\bar{A} + \bar{B}) \cdot \bar{C}$
 (d) $A + B \cdot C$

(ii) The universal gate is

- (a) NOR
- (b) AND
- (c) OR
- (d) EX-OR

(iii) The minimum number of two input NAND gates required to realize the function $(A\bar{B} + \bar{A}B)$ is

- (a) 5
- (b) 6
- (c) 4
- (d) 3

(iv) A byte organized memory chip has provision to accommodate 13, 42, 17, 728 number of bits. The organization of the chip is

- (a) $2^{10} \times 8$
- (b) $2^{24} \times 8$
- (c) $2^{20} \times 4$
- (d) $2^{24} \times 4$

(v) The simplified logic expression for $y = \bar{A}\bar{B} + A\bar{B} + AB$ is

- (a) AB
- (b) $\overline{A+B}$
- (c) $A+B$
- (d) $\bar{A} + \bar{B}$

(vi) The dual of $x \cdot \bar{x} = 0$ is

- (a) $\bar{x} + x = 0$
- (b) $x + \bar{x} = 1$
- (c) $\bar{x} \cdot x = 1$
- (d) $x + \bar{x} = 0$

(vii) Number of flip-flops needed to construct a mod-24 counter is

- (a) 2
- (b) 4
- (c) 5
- (d) 6

(viii) An asynchronous sequential circuit is

- (a) a combinational circuit with feedback.
- (b) a combinational circuit without feedback.
- (c) one that uses a clock.
- (d) None of the above.

(ix) In a synchronous sequential circuit, the present state designates the states of flip-flops

- (a) after the occurrence of the clock.
- (b) at the occurrence of leading edge of the clock.
- (c) before occurrence of the clock.
- (d) at the occurrence of falling edge of the clock.

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Group A

1. (a) Reduce the following function using Karnaugh map and implement using basic gates :

$$f(A, B, C, D) = \bar{A}\bar{B}D + A\bar{B}\bar{C}\bar{D} + \bar{A}BD + ABC\bar{D} \quad 10$$

- (b) Obtain the expression for the circuit output shown in Fig. 1. Simplify this expression and implement using basic gates : 10

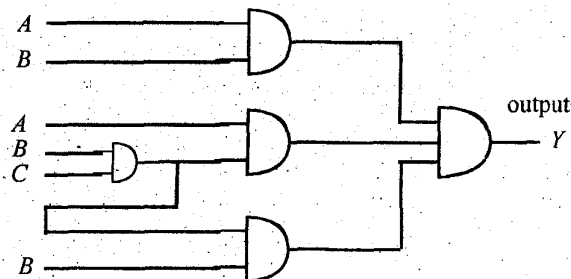


Fig. 1

2. (a) Convert following expressions to POS form: 2×3

(i) $Y = A(A + B)(A + B + C)$

(ii) $F = (A + B)(B + C)(A + C)$

(b) Reduce the following using Karnaugh map:

$f(A, B, C, D) = \pi m(0, 2, 3, 8, 9, 12, 13, 15)$

Express in POS form. 10

(c) Implement basic gates using (i) NAND gates only, and (ii) NOR gates only. $2+2$

3. (a) Write 4-to-1 line multiplexer logic diagram using NAND gates. Hence, realize the function $f(A, B, C) = \Sigma(1, 2, 6, 7)$ using the same. 10

(b) Convert to octal number $(68BE)_{16} = (?)_8$ 4

(c) Convert the following to decimal number: 2×3

(i) $(10110-0101)_2$

(ii) $(16-5)_{16}$

4. (a) Implement the following function using PLA: 10

$A(x, y, z) = \Sigma m(1, 2, 4, 6)$

$B(x, y, z) = \Sigma m(0, 1, 6, 7)$

$C(x, y, z) = \Sigma m(2, 6)$

(b) Simplify the following using tabular method: 10

$f(w, x, y, z) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15)$

$+ \Sigma d(4, 8, 11)$

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(Continued)

Group B

5. (a) Convert (i) SR flip-flop to D flip-flop, and (ii) JK flip-flop to T flip-flop. $5+5$

(b) Explain and design asynchronous MOD 10 counter using JK flip-flop. 10

6. (a) Design synchronous divide by 6 counter using T flip-flop. 8

(b) Design a 5 state sequential machine that gives 10001 as output sequence by choosing a suitable state transistor. 12

7. (a) Write and explain 4 bit up-down binary counter using T flip-flops, and show the state assignments used. 10

(b) Explain fault detection technique in sequential circuits with an example. 10

8. Write short notes on the following: 2×10

(a) Deterministic and non-deterministic recognisers.

(b) Regular expressions.

Group C

9. Choose the correct answer for the following: 10×2

(i) If $C = 0.01 \mu\text{F}$, $T = 100 \mu\text{s}$, then value of R in a monostable multivibrator is

(a) $1.43 \text{ k}\Omega$

(b) $14.3 \text{ k}\Omega$

(c) $143 \text{ k}\Omega$

(d) $1430 \text{ k}\Omega$

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(Turn Over)

(ii) Minimum number of flip-flops required to generate the sequence 1101011 is

- (a) 2
- (b) 3
- (c) 4
- (d) 5

(iii) Binary equivalent of $(306D)_{16}$ is

- (a) 001100001110-1011
- (b) 001000000110-1011
- (c) 001000000110-1101
- (d) 001100000110-1100

(iv) $A \cdot (A + B) =$

- (a) B
- (b) A
- (c) \bar{A}
- (d) None of the above

(v) Hexadecimal equivalent of $11111 + 10001$ is

- (a) 30
- (b) CO
- (c) FO
- (d) EO

(vi) 8421 code representation of $(62)_{10}$ is

- (a) 111110
- (b) 111111
- (c) 111101
- (d) None of the above.

(vii) $\bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC$ is equal to

- (a) A
- (b) B
- (c) C
- (d) None of the above

(viii) The excitation value, if $Q_n = 1$ and $Q_{n+1} = 0$ for JK flip-flop, is

- (a) $J=0, K=X$
- (b) $J=X, K=0$
- (c) $J=X, K=1$
- (d) $J=0, K=1$

(ix) 2-to-1 line multiplexer can be realized using

- (a) 1 NAND, 2 OR and 1 NOT gates
- (b) 2 NAND, 2 OR and 1 NOT gates
- (c) 2 NAND, 1 OR and 2 NOT gates
- (d) 2 NAND, 1 OR and 1 NOT gates

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Group A

1. (a) Realize a three-input AND gate using EX-OR gates. 10
 (b) Prove the following Boolean identities : 10
 (i) $AB + \bar{A}C + BC = AB + \bar{A}C$
 (ii) $AB + \bar{A}C = (A + C)(\bar{A} + B)$
2. (a) Differentiate between SOP and POS method of logic
 circuit design giving the basic difference between the
 two methods. Quote an example of each one of them. 8
 (b) Draw the NAND-NAND logic circuit using 3-inputs
 and four NAND gates to implement the function

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC$$
 where the symbols are fundamental products of an
 SOP circuit. Simplify the Boolean expression and
 explain whether the result is logical or not. 12

3. (a) Explain the utility of simplification of a Boolean expression using K-maps. Hence, explain the terms overlapping groups and rolling the map. 6
- (b) Reduce using mapping the expression:
 $\Pi M(2, 8, 9, 10, 11, 12, 14)$
 Draw the K-maps for both SOP and POS forms. Implement the more economical one using NOR gates. 14
4. (a) What are programmable logic arrays (PLA) and what is the basic operation carried out by it? Explain the operation of a PLA and the normal guidelines that are used in the design of a PLA taking a suitable example. 10
- (b) What is the advantage of the Quine-Mcclusky (QM) method of minimization of Boolean expression over K-maps? Explain the method of minimization by the QM method with a suitable example. What are prime implicants? Compare the limitations of K-map and QM method. 10

Group B

5. (a) State the steps you would follow in the synthesis of synchronous sequential circuits. Hence, explain how you would design a modulo-8 binary counter? Draw also its state transition and output tables. How does the design differ when the counter operation is in asynchronous mode? 10
- (b) Consider the SR flip-flop and draw the table for its excitation characteristics. Finally obtain the excitation requirements of the SR flip-flop using don't cares. Realize a D flip-flop from SR flip-flop. 10

6. (a) For binary inputs a, b and c , describe a finite state machine model for $y = a + b \oplus c$. 8
- (b) State the capabilities and limitations of finite state machines. Hence, prove that an n -state machine of a long sequence of 1s must have a period that cannot be greater than n . 12
7. (a) Write the steps that you would follow for the design of fundamental mode asynchronous sequential circuits. What are partial and primitive flow tables? Explain with reference to a suitable set of input-output sequence. 14
- (b) Describe the dependence of duty cycle on circuit components for a monostable multivibrator. 6
8. Write short notes on *any two* of the following: 10+10
- (a) Non-uniqueness of minimal machines
- (b) Finite state recognizers.
- (c) T and D flip-flops realization using NOR gates.

Group C

9. Choose the *correct* answer for the following: 10 × 2
- (i) The exclusive X-OR operation on variables A and B is denoted by
- (a) $(AB + \bar{A}\bar{B})$
- (b) $(A\bar{B} + \bar{A}B)$
- (c) $(AB + \bar{A}\bar{B})$
- (d) $(AB + \bar{A}B)$

(ii) The variable A can be written as

- (a) $(A + B\bar{B})$
- (b) $(B + A)(B + \bar{A})$
- (c) $(AB + \bar{A}\bar{B})$
- (d) $(B + A\bar{A})$

(iii) What is the value of b in the conversion $16_{10} = 100_b$?

- (a) 2
- (b) 8
- (c) 6
- (d) 4

(iv) How many possible combinations of input variables exist in a 4-variable expression?

- (a) 8
- (b) 10
- (c) 16
- (d) 24

(v) Which one of the following symbol is not used in a *don't care* in majority of texts:

- (a) d
- (b) X
- (c) ϕ
- (d) n

(vi) What is the maximum number of variables that can be used in the minimization of a K-map?

- (a) 4
- (b) 6
- (c) 8
- (d) 10

(vii) The equivalent name for multiplexer is

- (a) multi
- (b) data encoder
- (c) data selector
- (d) demux

(viii) Permanent faults in combinational circuits are due to

- (a) parity bit
- (b) noise
- (c) component failure
- (d) low supply voltage

(ix) Which one of the following operation cannot be performed by flip-flops?

- (a) data storage
- (b) data transfer
- (c) adder
- (d) counting

S' 10 : 5 AN : CP 405/EC 422 (1450)

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Group A

1. (a) State and prove De Morgan's theorems. 6
- (b) (i) $(ABCD)_{16} = (?)_{10}$ 2
- (ii) $(10101111)_2 = (?)_8$ 2
- (c) Simplify the following using K-map :

$$f(A,B,C,D) = \sum m(7, 8, 9) + \sum d(10, 11, 12, 13, 14, 15).$$
 10
2. (a) A truth table has a low output for the first three input conditions: 000, 001 and 010. If all other outputs are high, what is the product-of-sum (POS) form represented by the truth table ? 4

(b) Define minterms and maxterms. Express $f = A + \bar{B}C$ as a sum of minterms. 6

(c) Minimise the function $f = \sum m(0, 2, 3, 6, 7, 8, 9, 10, 13)$ using Quine McClusky method. 10

3. (a) Implement the function $f = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + ABC\bar{D} + A\bar{B}C\bar{D} + \bar{A}BC\bar{D}$ using a 8 to 1 multiplexer with A, B and D as select inputs. 10

(b) Implement the following function using PLA: 10
 $f(x, y, z) = \sum m(0, 1, 3, 5)$
 $g(x, y, z) = \sum m(2, 4, 6)$
 $h(x, y, z) = \sum m(4, 7)$

4. (a) Write a note on read only memories. 6
 (b) Briefly discuss about various types of faults that occur in digital circuits. 6
 (c) Find the Boolean difference with respect to x_2 in the following circuit: 8

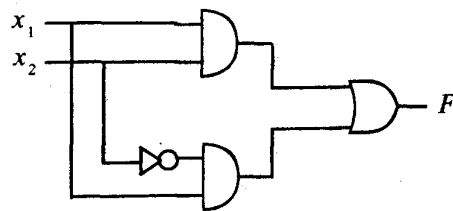


Fig.1

Group B

5. (a) Explain the working of a master-slave JK flip-flop. 10
 (b) Design an asynchronous mod 9 counter using JK flip-flop. 10

6. (a) Design a counter with the following repeated binary sequence 0, 1, 3, 5, 7. Use T flip-flops. 14
 (b) Define the following terms: 3 x 2

- (i) Finite-state machine
- (ii) Incompletely specified machine
- (iii) Compatible states.

7. (a) Design a pulse mode asynchronous sequential circuit that has two inputs X_1 and X_2 , one Mealy output Z_1 and one Moore output Z_2 . The Mealy output is coincident with the third consecutive pulse on input X_2 and the Moore output occurs after the third consecutive pulse on input X_2 or after any pulse that occurs on input X_1 . 16

(b) Define fundamental mode circuit and pulse mode circuit. 2+2

8. Write notes on the following: 5+10+5

- (a) Deterministic recognisers
- (b) Graphs
- (c) Regular expressions.

Group C

9. Choose the *correct* answer for the following: 10×2

(i) $A + \bar{A}B$ is

(a) A

(b) B

(c) $A + B$

(d) $\bar{A} + \bar{B}$

(ii) $\frac{\bar{A} + \bar{B}C}{\bar{A} + \bar{B}C}$ is

(a) $A + B + C$

(b) ABC

(c) $A + \bar{B}\bar{C}$

(d) $A \cdot (\bar{B} + \bar{C})$

(iii) In $(0.3125)_{10} = (x)_2$, the value of x is

(a) 0.0101

(b) 0.1010

(c) 0.1001

(d) 0.0010

(iv) The canonical sum of product form of the function

$F = A + B$ is

(a) $AB + A\bar{B} + \bar{A}B$

(b) $AB + BA$

(c) $AB + A\bar{B}$

(d) $A\bar{B} + \bar{A}B$

(v) The canonical product of sum form of $F = (A + \bar{B})(B + C)$ is

(a) $(A + \bar{B} + C)(A + \bar{B} + \bar{C})$

(b) $(A + \bar{B} + C)(A + \bar{B} + \bar{C})(A + B + C)$
 $(\bar{A} + B + C)$

(c) $(A + \bar{B} + C)(A + \bar{B} + \bar{C})(A + B + C)$

(d) $(A + \bar{B} + \bar{C})(\bar{A} + B + C)$

(vi) The JK flip-flop acts as a T flip-flop, when

(a) $J = 1, K = 0$

(b) $J = 0, K = 0$

(c) $J = 1, K = 1$

(d) $J = 0, K = 1$

(vii) The number of T flip-flops required to realise a mod-5 counter is

(a) 3

(b) 5

(c) 2

(d) 10

(viii) The number of states of a cyclic mod-8 synchronous binary counter is

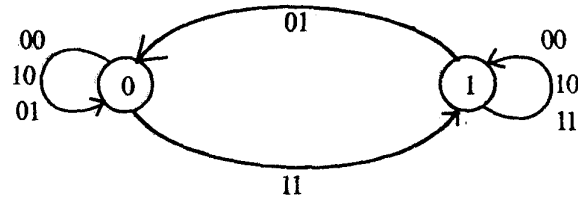
(a) 3

(b) 8

(c) 2

(d) 64

- (ix) The state diagram of an asynchronous sequential circuit is shown below :



The number of outputs of the circuit is

- (a) 2
 - (b) 4
 - (c) 6
 - (d) 1
- (x) The number of inputs of the circuit depicted by the state diagram, shown in question 9(ix) above, is
- (a) 2
 - (b) 4
 - (c) 6
 - (d) 1

W' 10 : 5 AN : CP 405/EC 422 (1450)

PULSE AND DIGITAL CIRCUITS

Time : Three hours

Maximum Marks : 100

Answer FIVE questions, taking ANY TWO from Group A, ANY TWO from Group B and ALL from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answers may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification.

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) What do you mean by universal logic gates? Name universal gates. Justify your answer. Design the logic $A + BC + \bar{A}\bar{C}$ using only NAND gates. 10
- (b) Convert the following:
 - (i) $X = ABC + AD$ into SOP format
 - (ii) $Y = (A + B + C)(A + D)$ into POS format.

Also, minimize the function $X + Y$ for Boolean X and Y . 10
2. (a) If $X = 1010100$ and $Y = 1000011$, find $(X - Y)$ and $(Y - X)$ using (i) 1s complement method, and (ii) 2s complement method. Also, give a design to have $X.Y$, where '.' represents a binary multiplication. 10

(b) Simplify the following using Boolean algebra : 3+3+4

(i) $X = \overline{A+B+C} + (B+\overline{C})(\overline{B}+C)$

(ii) $Y = \overline{A\overline{B}(CD+EF)}(\overline{A\overline{B}} + \overline{CD})$

(iii) $Z = A\overline{B} + \overline{A}B$

3. (a) Implement the following two Boolean functions with a PLA: 5+5

$F_1(A, B, C) = \Sigma(0, 1, 2, 4)$

$F_2(A, B, C) = \Sigma(0, 5, 6, 7)$

(b) Simplify the following using K-map:

$F(A, B, C, D, E) = \Sigma(0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$

Implement using only NAND gates. 10

4. (a) Minimize the following using Tabular method: 10

$Y = \overline{A}B\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} + A\overline{B}C\overline{D} + A\overline{B}C\overline{D} + A\overline{B}C\overline{D} + \overline{A}\overline{B}C\overline{D}$

(b) What is static 0, static 1 and dynamic hazard? What are the conditions for arising of such hazards? What are the steps followed in detecting and eliminating static and essential hazards? 10

Group B

5. (a) Design synchronous MOD-10 BCD up-down counter using T-flipflops and other gates. 10

(b) Describe the race around problem in J-K flipflop. 10

6. (a) Draw the state diagram, state table, and algorithmic state machine chart for a sequence detector to detect the sequences 1111 and 0000. Overlapping is not allowed. 10

(b) How can you design a 4-state machine to get a desired input/output sequence pair? 10

7. (a) What are the conditions for two machines to be equivalent? For the machine shown in state table below, find reduced machine in standard form: 10

PS	NS, Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

(b) Convert the following: 5+5

(i) SR to J-K flipflop

(ii) D to S-R flipflop.

8. (a) Design a 3-bit odd parity generator using J-K flipflop. 10

(b) How can a non-deterministic graph be converted into a deterministic graph? 10

Group C

9. Choose most suitable answer for the following: 10×2

(i) $\overline{A}B\overline{C}\overline{D} + B\overline{C}\overline{D} + B\overline{C}\overline{D} + B\overline{C}\overline{D} =$

(a) $\overline{B}(\overline{D} + \overline{C})$

(b) $\overline{B} + \overline{D} + \overline{C}$

(c) $B(\overline{D} + \overline{C})$

(d) $\overline{B}(D + C)$

(ii) For even number of ones at the inputs, the output of EX-NOR gate is

- (a) low.
- (b) high.
- (c) oscillating.
- (d) None of the above.

(iii) $(13.125)_{10} = (?)_8$

- (a) 3.7
- (b) 16.5
- (c) 15.1
- (d) 15.5

(iv) $(6AOC)_{16} = (?)_{10}$

- (a) 27148
- (b) 27814
- (c) 27184
- (d) 21748

(v) Multiplexer can be expressed as

- (a) one-to-many.
- (b) many-to-one.
- (c) many-to-many.
- (d) one-to-one.

(vi) Tabular method of simplification is convenient as long as the number of variables does not exceed

- (a) 6
- (b) 8
- (c) 10
- (d) 12

(vii) If $L = \text{low}$, $H = \text{high}$, a positive logic is

- (a) $L = 5V, H = 0V$
- (b) $L = 5V, H = -5V$
- (c) $L = 5V, H = 1V$
- (d) $L = -5V, H = -1V$

(viii) If input and output of a NOT gate is shorted, then output will be

- (a) 0
- (b) 1
- (c) a pulse.
- (d) indeterminant.

(ix) The characteristic equation of a T flipflop is

- (a) $T \oplus Q_n$
- (b) $T + Q_n$
- (c) TQ_n
- (d) None of the above

(x) The minimum number of flipflops (n) required to generate a sequence of length, N , should satisfy

(a) $N \geq 2^n - 1$

(b) $n \geq 2^N - 1$

(c) $N \leq 2^n - 1$

(d) $n \leq 2^N - 1$

S'11 : 5 AN : CP 405/EC 422 (1450)

PULSE AND DIGITAL CIRCUITS

Time : Three hours

Maximum Marks : 100

*Answer FIVE questions, taking ANY TWO from Group A,
ANY TWO from Group B and ALL from Group C.*

*All parts of a question (a, b, etc.) should be
answered at one place.*

*Answer should be brief and to-the-point and be supple-
mented with neat sketches. Unnecessary long answers
may result in loss of marks.*

*Any missing or wrong data may be assumed suitably
giving proper justification.*

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Verify that a set of ANDed inputs A, B, C, \dots is equivalent to the inverse of the ORed inputs $\bar{A}, \bar{B}, \bar{C}, \dots$. Derive De Morgan's laws from this Boolean equation and explain the duality involved. 6
- (b) Transform the following: 3+3
 - (i) $(10100110101111)_2 = (\text{---})_{16}$
 - (ii) $(A72E)_{16} = (\text{---})_8$.
- (c) Prove the following Boolean identities: 4+4
 - (i) $A + \bar{B}C(A + \bar{B}C) = A + \bar{B}C$
 - (ii) $A + B[AC + (B + \bar{C})D] = A + BD$.

2. (a) Reduce the expression using K-map in SOP and POS forms.

$$\sum m(1, 5, 6, 12, 13, 14) + d(2, 4)$$

Also, implement the minimal expression in universal logic. 10

- (b) Obtain the set of prime implicants for $\sum m(0, 1, 6, 7, 8, 9, 13, 14, 15)$ using binary designation of minterms. 10

3. (a) What is a 'switching function'? Give some of the basic properties of switching functions and show that a switching function $T_1(x, y, z)$ is identical with $T_2(x, y, z)$ if $T_1 = x'z + xz' + x'y'$ and $T_2 = x'z + xz' + y'z'$. 8

- (b) Prove the following identity: $xy + x'y' + yz = xy + x'y' + x'z$ 6

- (c) Simplify the expression $T(A, B, C, D) = A'C' + ABD + BC'D + AB'D' + ABCD'$. 6

4. (a) Write briefly about permanent and transient faults in combinational circuits. Hence, explain the terms equivalent and distinguishable faults. 8

- (b) State and explain the Boolean differences method for determining the complete set of tests that can detect a given fault. What is the condition that a set of tests which detects a fault $x_i s - a - 0$ and $x_i s - a - 1$? 8

- (c) Briefly explain the basic principles of fault detection by path sensitising. 4

Group B

5. (a) Draw the K-map of an S-R and J-K flip-flop. Use don't cares for intermediate steps. Hence, show that the characteristic equation for an S-R flip-flop of the form $Q_{n+1} = S + R'Q_n$. 12

- (b) What are Finite State Machines and how are they more useful than truth tables in understanding the operation of a sequential circuit? Draw the state transition diagram of an S-R and J-K flip-flop, briefly explaining the input and output variables. 8

6. (a) Give the steps you would follow for designing sequential circuits using various types of memory elements. Draw the block diagram of a serial binary adder and generate its state table. 10

- (b) State the basic difference between a Mealy and a Moore model for representing a state diagram. Use the example of a D-flip-flop to illustrate this. Also, draw the related excitation table. 10

7. (a) What are asynchronous sequential circuits and their advantages? Draw the block diagram of such a circuit using the basic model for the fundamental mode circuit and explain its operation with reference to stable and unstable states. 12

- (b) The AND gate, shown in Fig. 1 below, has an input A and a feedback input x with delay time ' τ '. Draw the K-map for the circuit and analyze the condition for stability of a state. 8

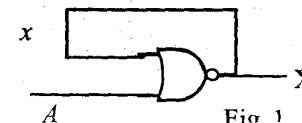


FIG 1

8. Write short notes on *any two* of the following: 10+10

- (a) Divide by seven counter
- (b) Monostable multivibrator
- (c) Schmidt trigger.

Group C

9. Choose the *correct* answer for the following: 10 × 2

(i) $A + A.B$ is equal to

- (a) $A + B$
- (b) $\bar{A} + \bar{B}$
- (c) A
- (d) $A + 1$

(ii) $(A + \bar{B})(C + \bar{D})$, when deorganized, gives

- (a) $A.\bar{B} + C.\bar{D}$
- (b) $A.\bar{B} + \bar{C}.D$
- (c) $\bar{A}.B + \bar{C}.D$
- (d) $\bar{A}.B + C.\bar{D}$

(iii) Convert $(110101.101010)_2$ to octal. The answer is

- (a) 65.52_8
- (b) 56.25_8
- (c) 65.57_8
- (d) 65.75_8

(iv) The output Y of the circuit shown in Fig. 2 is



Fig. 2

- (a) $\bar{A}\bar{A}$
- (b) A
- (c) 1
- (d) \bar{A}

(v) The output Y of a NOR gate for inputs A and B is

- (a) $\bar{A} + \bar{B}$
- (b) $\overline{A + B}$
- (c) $\bar{A} + \bar{B}$
- (d) \overline{AB}

(vi) How many AND gates are required to decode eight possible input states of a PLA with 3 input variables and 3 output variables?

- (a) 6
- (b) 4
- (c) 8
- (d) 2

(vii) Hazards in switching circuits are caused by

- (a) varying input signal.
- (b) constant output.
- (c) zero propagation time.
- (d) delays of switching components.

- (viii) Which condition below is normally not used in an S-R flip-flop?
- (a) $S = 0, R = 0$.
 - (b) $S = 1, R = 0$.
 - (c) $S = 1, R = 1$.
 - (d) $S = 0, R = 1$.
- (ix) Specification of a synchronous sequential machine is given by its
- (a) initial state.
 - (b) final state.
 - (c) stable state.
 - (d) state table.
- (x) In a transition graph, a set of directed graphs is referred to as
- (a) path.
 - (b) line.
 - (c) arc.
 - (d) track.

W' 11:5 AN:CP 405/EC 422 (1450)**PULSE AND DIGITAL CIRCUITS***Time : Three hours**Maximum Marks : 100*

Answer FIVE questions, taking ANY TWO from Group A, ANY TWO from Group B and ALL from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answers may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) State and prove De Morgan's theorem. What are minterms and maxterms? Give an example for each. 5
- (b) Design a Boolean logic expression for full adder. 10
- (c) Find $X \oplus Y$ using 1s complement and 2s complement methods for $X = 11011011$ and $Y = 10101010$. 5
2. (a) Simplify the following Boolean expression using Karnaugh map method. Implement the simplified expression using NAND gates only : 12
 $f = \sum m(0, 1, 2, 5, 7, 9, 12, 14, 21, 23, 26, 29)$
 $+ \sum d(6, 15, 28, 30, 31)$

- (b) Define the term “don’t care combination” in Boolean logic circuits. 8
3. (a) Reduce the following function using Quine McClusky method. Implement the reduced function using NAND gates only : 10
- $$f = \sum m(1, 3, 4, 7, 9, 11, 12, 14) + \sum d(2, 6, 13)$$
- (b) Describe a 4×1 digital multiplexers and indicate the clocks at various stages. 10
4. (a) Explain briefly about various types of hazards in combinational circuits. How can hazard-free designs be worked out ? 8
- (b) Explain fault diagnosis by path sensitization method taking an appropriate example. Compare its merits with that of Boolean difference method. 12

Group B

5. (a) Explain the design of master slave J-K flip-flop with NOR gates and discuss the race around program. 12
- (b) Realize a D flip-flop with T flip-flop. 6
- (c) Give an application of a monostable multivibrator. How can it be designed with user specific choice of pulse characteristic ? 2
6. (a) Design a synchronous mod-13 up-down counter using J-K flip-flops. 12

- (b) Explain the following terms : 4 × 2
- (i) Synchronous sequential circuit
 (ii) Fundamental mode circuit
 (iii) Pulse mode circuit
 (iv) Finite-state machine

7. (a) Design a fundamental mode asynchronous sequential circuit that has two inputs, X_1 and X_2 , and one output z . When $X_1 = 0$, the output $z = 0$. The first change in X_2 that occurs while $X_1 = 1$ will cause output z to be 1. The output z will remain 1 until X_1 return to 0. 16
- (b) What is the difference between completely specified and incompletely specified machines ? 4

8. Write notes on the following : 10 + 10
- (a) Deterministic recognisers
 (b) State assignments in asynchronous sequential circuits.

Group C

9. Choose the *correct* answer for the following : 10 × 2
- (i) The dual of $x(y'z' + yz)$ is
- (a) $x + (y' + z')(y + z)$
 (b) $x \cdot (y' + z') + (y + z)$
 (c) $x + (y'z' + y + z)$
 (d) $x + y'z' + yz$

(ii) $x(x + y) =$

- (a) $x + y$
- (b) x
- (c) $1 + x$
- (d) y

(iii) The number of select lines needed in a 8×1 multiplexer is

- (a) 8
- (b) 3
- (c) 2
- (d) 1

(iv) A $(2^k \times n)$ ROM will have

- (a) k inputs and n outputs.
- (b) 2 inputs and n outputs.
- (c) k outputs and n inputs.
- (d) 2^k inputs and n outputs.

(v) A PLA is

- (a) programmable AND array, programmable OR array.
- (b) programmable AND array, fixed OR array.
- (c) fixed AND array, fixed OR array.
- (d) fixed AND array, programmable OR array.

(vi) Which one of the following is true with respect to flip-flops?

- (a) $D = J'Q' + K'Q$
- (b) $D = JQ' + K'Q$
- (c) $D = JQ + KQ'$

(vii) The minimum number of flip-flops required to realise a mod 3 counter is

- (a) 3
- (b) 8
- (c) 2
- (d) 6

(viii) When $J = K = 1$ in a J-K flip-flop, the output is

- (a) set.
- (b) reset.
- (c) goes to tristate.
- (d) toggles.

(ix) The number of states in a divide by N counter is

- (a) $N - 1$
- (b) 2^{N-1}
- (c) $2^N - 1$
- (d) N

(x) In a primitive flow table, the number of stable total state in each row is

- (a) 1
- (b) 2
- (c) 3
- (d) 4

S'12:5 AN: CP 405/EC 422 (1450)

PULSE AND DIGITAL CIRCUITS

Time : Three hours

Maximum Marks : 100

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mented with neat sketches. Unnecessary long answer may
result in loss of marks.*

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giving proper justification.*

Figures on the right-hand side margin indicate full marks

Group A

1. (a) Transform the following : 3 × 3
- (i) $(6715)_8 = (---)_{10}$
- (ii) $(6A0C)_{16} = (---)_{10}$
- (iii) $(238)_{10} = (---)_{16}$
- (b) (i) Convert $(A + B + C).(A + D)$ into POS format. 3
- (ii) Convert $A.B.C + A.D$ into SOP format.
Do not use Karnaugh map. 3
- (c) Implement $\pi M (0,1,2,3,10,11)$ using only NOR
gates in simplified form. 5

(Turn Over)

2. (a) Identify the function $Y = \sum M(1, 2, 4, 7, 8, 11, 13, 14)$ in simplest form and implement using only three logic gates. 10
- (b) Simplify using Karnaugh map and implement using minimum logic gates :
 $F = f(a, b, c, d, e) = \sum m(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25, 27, 28, 30)$ 10
3. (a) Using Quine-McClusky method, reduce $Y = f(a, b, c, d) = \sum M(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$ and implement using NAND gate only. 10
- (b) Multiply the following using 4:1 multiplexers :
 (i) $F_1 = \sum m(3, 7, 9, 10)$
 (ii) $F_2 = \sum m(2, 7, 12, 15)$
 (iii) $F_3 = \sum m(3, 7)$ 3 + 3 + 4
4. (a) Implement $F(a, b, c) = \sum m(0, 5, 6, 7)$ using PLA. 10
- (b) Design a ROM-based circuit which converts 3-bit binary to excess-3 code. 10

Group B

5. (a) With the help of a logic diagram and truth table, explain the working of a J-K flip-flop. Derive its characteristic equation. What do you mean by 'race-around' condition? How is it removed? 10
- (b) Design a divide-by-8 counter using J-K flip-flop. Extend it to 4-bit Johnson counter. 10
6. (a) Design a sequence detector which detects occurrence of sequence 1010. Overlapping is allowed. Use D flip-flop. 14

S'12 : 5 AN : CP 405/EC422 (1450) (2)

(Continued)

- (b) Convert (i) S-R flip-flop to J-K flip-flop, and (ii) J-K flip-flop to T flip-flop by using the respective truth table relations. 6
7. (a) Design a synchronous gray code up-counter using J-K flip-flops. 20
8. (a) An unknown one-input three-state machine produces an output Z for input X as follows :
- X: 0 0 0 0 1 0 1 0 0 0 1 0
 Z: 1 0 1 0 0 1 1 0 0 0 0 1
- If A is initial state, find reduced standard form of machine. 10
- (b) Find transition graph that recognizes the strings : 5 + 5
 (i) $(0 + 1)(11 + 0^*)^*(0 + 1)$
 (ii) $(0 + 11)^*(1 + (00)^*)^*11$

Group C

9. Choose the correct answer for the following : 10 × 2
- (i) $(9AF27)_{16} + (ABCD4)_{16} = (-)_{16}$
 (a) 156 FFB
 (b) 156 BBF
 (c) 146 BFB
 (d) 146 FFB
- (ii) If $(292)_{10} = (1204)_B$, where B is
 (a) 2
 (b) 4

S'12 : 5 AN : CP 405/EC422 (1450) (3)

(Turn Over)

- (c) 6
(d) 8
- (iii) $\bar{w}\bar{x} + \bar{x}\bar{y} + \bar{w}\bar{z} + \bar{y}\bar{z} = (?)$
 (a) $\bar{x}\bar{y} + \bar{w}\bar{x}$
 (b) $\bar{x}\bar{y} + \bar{w}\bar{z} + yz$
 (c) $\bar{w}\bar{z} + yz$
 (d) $\bar{w}\bar{z} + \bar{x}\bar{y}$
- (iv) Minimal SOP form of $F = \sum m(0,1,2,3,4,6,8,9,10,11)$ is
 (a) $\bar{x}\bar{z} + \bar{w}$
 (b) $\bar{x} + \bar{w}\bar{z}$
 (c) $\bar{x} + \bar{z} + \bar{w}$
 (d) $\bar{x}\bar{w}\bar{z}$
- (v) The sum of ripple carry adder is
 (a) $S_i = A_i \oplus B_i \oplus C_i$
 (b) $S_i = A_i B_i + A_i C_i + B_i C_i$
 (c) $S_i = A_i + B_i + C_i$
 (d) $S_i = A_i B_i C_i$
- (vi) A 4-bit up-down counter is in down mode and PS = 1100. The NS will be
 (a) 1011
 (b) 0111
 (c) 1110
 (d) 1101
- (d) 1101
- (vii) For Mod-32 counter, number of flip-flops required is
 (a) 4
 (b) 5
 (c) 8
 (d) 3
- (viii) An n -bit ring counter is a mod— counter, whereas an n -bit twisted ring counter is a mod— counter, respectively.
 (a) $2n, n$
 (b) $n, 2n$
 (c) n, n
 (d) $2n, 2n$
- (ix) A PLA
 (a) is field programmable.
 (b) is mask programmable.
 (c) can be programmed by the user.
 (d) can be erased and programmed.
- (x) — lines are contained in a multiplexer with 1024 inputs and one output.
 (a) 512
 (b) 258
 (c) 64
 (d) 10

W' 12: 5 AN: CP 405/EC 422 (1450)**PULSE AND DIGITAL CIRCUITS***Time : Three hours**Maximum Marks : 100*

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Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Write important postulates of Boolean algebra. How is it different from conventional algebra? 5
- (b) How is dual of a Boolean expression obtained? Explain by giving a suitable example. 5
- (c) State and prove De-Morgan's theorem. 5
- (d) State and prove Transposition theorem. 5
2. (a) Define (i) product-of-sums (POS) form, and (ii) sum-of-products (SOP) form. 3 + 3
- (b) What is the difference between canonical form and standard form? Which form is obtained from a truth table? 6

- (c) Prove that the sum and product of all minterms of a Boolean function of three variables is 1 and 0, respectively. 4
- (d) Consider a 3-bit binary numbers $X_3 X_2 X_1$, where X_1 is LSB. Design a circuit that will determine whenever the binary is greater than 4. 4
3. (a) Minimize the following switching functions using Karnaugh map. List all prime implicants and essential prime implicants (non-redundant group):
- (i) $F = \sum (1, 3, 5, 6, 7)$
- (ii) $F = \sum (0, 1, 3, 6, 14, 15)$ 8
- (b) Simplify the following Boolean functions by Quine-McCluskey, method: (i) $F = \sum (1, 3, 5, 8, 10, 14)$, and (ii) $F = \sum (1, 9, 10, 16, 20) + \sum_{d'} (14, 29, 30)$, 12
4. (a) How does a programmable logic device differ from a fixed logic device? What are the primary advantages of using programmable logic devices? 6
- (b) Distinguish between a programmable logic array (PLA) device and a programmable array logic (PAL) device in terms of architecture and capability to implement Boolean functions. 6
- (c) Determine the size of the PROM required for implementing the following logic circuits: 8
- (i) A binary multiplier that multiplies two four-bit numbers;
- (ii) A dual 8-to-1 multiplexer with common selection inputs; and
- (iii) A single-digit BCD adder/subtractor with a control input for selection of operation.
- Group B**
5. (a) What are the differences between combinational and sequential logic circuits? 5
- (b) Explain following terms with diagram: (i) Clocked SR flip-flop, (ii) Clocked J-K flip-flop, and (iii) Clocked D flip-flop. 3 + 3 + 3
- (c) With the help of a suitable circuit, briefly explain how a D flip-flop can be used to detect the sequence of occurrence of edges of synchronous inputs. 6
6. Design a synchronous counter using J-K flip-flop that counts as 000, 010, 101, 110, 000, 010, Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. What will be the counter hardware look like if the unused states are to be considered as 'don't care's'. 20
7. (a) What is the difference between synchronous and asynchronous counters? 3
- (b) Explain, with a neat diagram, the working of a ripple counter. 5
- (c) Design asynchronous decade up/down counter. 12
8. (a) Design a deterministic finite automata to recognize strings of $\sum = \{0, 1\}$ such that it starts and end with 010 and 011, respectively. 5
- (b) Prove that for every NFA there exists a DFA. 5
- (c) Define regular expression. Write the regular expression that represents strings of $\sum = \{0, 1\}$ and

contains '01' as a substring. Convert this regular expression to a DFA. 10

Group C

9. Choose the *correct* answer for the following : 10 × 2

- (i) A ring counter consisting of five flip-flops will have
- 5 states
 - 10 states
 - 32 states
 - infinite states.
- (ii) When simplified with Boolean algebra, $(x+y)(x+z)$ simplifies to
- x
 - $x + x(y+z)$
 - $x(1+yz)$
 - $x + yz$
- (iii) If the input to T-flip-flop is 100 Hz signal, the final output of three T-flip-flops in cascade is
- 1000 Hz
 - 500 Hz
 - 333 Hz
 - 12.5 Hz
- (iv) A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be
- 15 ns

- 30 ns
- 45 ns
- 60 ns

(v) Words, having 8-bits, are to be stored into computer memory. The number of lines required for writing into memory is

- 1
- 2
- 4
- 8

(vi) How many flip-flops are required to construct mod 30 counter ?

- 5
- 6
- 4
- 8

(vii) Karnaugh map is used for the purpose

- of reducing the electronic circuits used.
- to map the given Boolean logic function.
- to minimize the terms in a Boolean expression.
- to maximize the terms of a given Boolean expression.

- (viii) Select the incorrect statement from the following.
- (a) $FA \subseteq LBA \subseteq TM$
 - (b) $LBA \subseteq TM$
 - (c) $LBA \subseteq PDA \subseteq TM$
 - (d) $FA \subseteq PDA \subseteq LBA$
- (ix) Select the incorrect statement to the regular expression $011(0+1)^*101$:
- (a) String of '0' and '1'.
 - (b) String starts with 011.
 - (c) Smallest string represented by the regular expression is 011101.
 - (d) Largest string represented by the regular expression is 01101101.
- (x) Mealy and Moore machines are
- (a) known as transducers.
 - (b) equivalent to each other.
 - (c) differentiated by the method to produce output.
 - (d) None of the three above.

S'13 : 5 AN : CP 405/EC 422 (1450)

PULSE AND DIGITAL CIRCUITS

Time : Three hours

Maximum Marks : 100

Answer FIVE questions, taking ANY TWO from Group A, ANY TWO from Group B and ALL from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

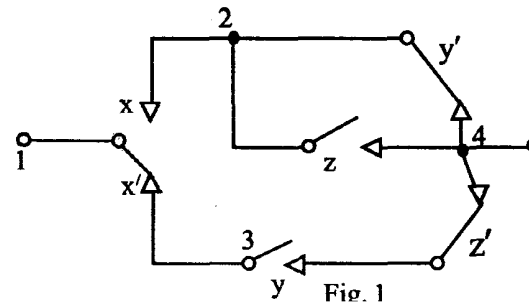
Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answer may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification.

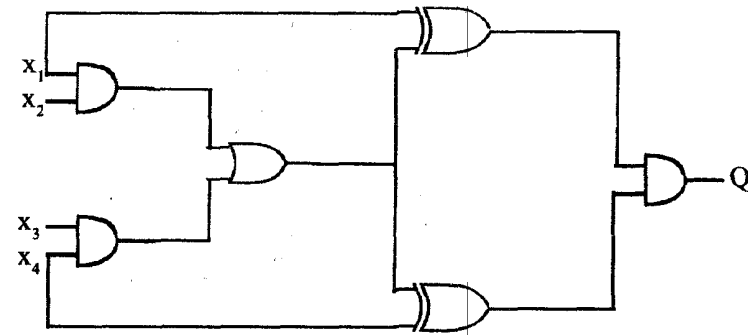
Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Realize Boolean $y = a + \bar{a}b$ using a single logic gate. 5
- (b) State and prove De Morgan's law and realize the Boolean function of question 1(a) using only NAND gates. 8
- (c) Compute the Boolean function of the following contact network. Write the truth table of it. Also, minimize the function, if possible. 7



2. (a) What is a self-dual function ? Give an example to explain. 4
- (b) What are functionally complete sets ? Give two examples. 6
- (c) State *any four* identities of exclusive-OR operation. Show that parallel combination of EX-OR with AND gate is a simple OR gate. 4
- (d) Define the following : 3 × 2
- (i) Karnaugh map
- (ii) Quine McCueky table
- (iii) Negative OR logic gate
3. (a) Minimize the following switching function using Karnaugh map method. Implement the function using NAND gates only. 10
- $$f(A, B, C, D, E) = \sum m(0, 1, 4, 9, 11, 16, 22, 25, 31) + \sum d(3, 10, 24, 30)$$
- (b) Design a 4 to 1 multiplexer using 2 × 1 multiplexers and explain its functions. 5
- (c) Describe a PLA and give an example of 3-variable Boolean function implementation with PLA. 5
4. (a) Design a 3-bit adder using suitable logic gates. 10
- (b) Write an expression for the output of the circuit shown below : 6

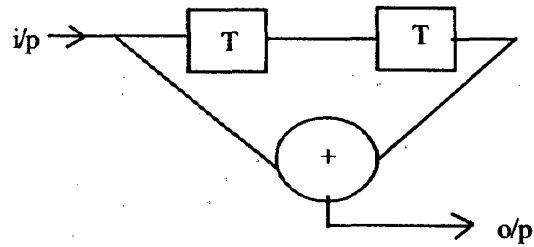


- (c) What is ROM ? If it is not a sequential circuit, how does it represent a memory ? 4

Group B

5. (a) Design and explain the working of a master-slave J-K flip-flop. Show that $Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$ represents J-K flip-flop. 10
- (b) Design asynchronous mod-6 counter and explain its working. 10
6. (a) Define the following terms : 4 × 2
- (i) Latch
- (ii) Flip-flop
- (iii) Synchronous counter
- (vi) Racearound
- (b) Convert (i) S-R flip-flop to D flip-flop, and (ii) S-R flip-flop to J-K flip-flop. 6 + 6
7. (a) An asynchronous sequential machine has two input terminals. It produces an output whenever 10 occur in one input line and 01 is present on the other input line. Construct a circuit for this logic. 10

(b) Write a state transition table for the following digital circuit: 10

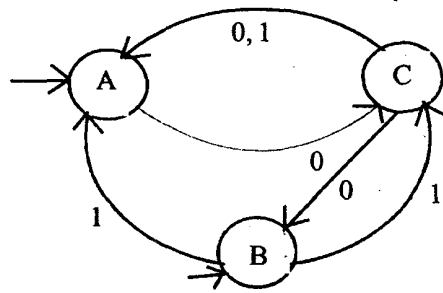


8. (a) Construct the graphs that recognise the following regular sets: 6 + 6

(i) $(01 + (11 + 0)1^*0)^*11$

(ii) $(1(00)^*1 + 01^*0)^*$

(b) Is the following graph a deterministic one? If not, then convert it to a deterministic one: 8



Group C

9. Answer the following: 10 × 2

(i) For a 16-bit binary code, parity check can be obtained with at least

(a) 4-bits

(b) 3-bits

(c) 2-bits

(d) 1-bit

(ii) The decimal numbers 510 can be represented in binary coded decimal with

(a) 12-bits

(b) 10-bits

(c) 19-bits

(d) 8-bits

(iii) The Boolean expression

$$Q = (x + y)(x + yz) + x'y' + x'z'$$

(a) $x + y$

(b) $xy + \bar{y}$

(c) 1

(d) $xyz + x'z'$

(iv) A PLA is sa

(a) AND-OR structure.

(b) NAND-EXOR structure.

(c) AND-AND structure.

(d) OR-OR structure.

(v) A non-universal logic gate is

(a) EX-NOR

(b) NAND

(c) AND

(d) EX-OR

(vi) Any 2^n to 1 multiplexer can be implemented by number of control bits at least

(a) 1

(b) $n - 1$

(c) n

(d) $n + 1$

(vii) The characteristic equation of a J-K flip-flop is

(a) $JQ' + K'Q$

(b) $JQ + K'Q'$

(c) $J + KQ$

(d) $J' + K'Q$

(viii) The number of flip-flops required to realise a mod 9 counter is

(a) 9

(b) 3

(c) 4

(d) 10

(ix) Choose the correct statement :

(a) Latch has race problem.

(b) J-K flip-flop is always synchronous.

(c) S-R flip-flop is always integrating.

(d) ROM is not a memory.

(x) Dual Boolean functions A and B satisfy

(a) $A(\bar{x}) = B(x)$

(b) $A(x) = \bar{B}(\bar{x})$

(c) $A(\bar{x}) = \bar{B}(x)$

(d) $A(\bar{x}) = B(\bar{x})$

W'13 : 5 AN : CP 405/EC 422 (1450)**PULSE AND DIGITAL CIRCUITS***Time : Three hours**Maximum Marks : 100**Answer FIVE questions, taking ANY TWO from Group A, ANY TWO from Group B and ALL from Group C.**All parts of a question (a, b, etc.) should be answered at one place.**Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answer may result in loss of marks.**Any missing or wrong data may be assumed suitably giving proper justification.**Figures on the right-hand side margin indicate full marks.***Group A**

1. (a) With the help of De' Morgan's law statement, realize the function

$$y = x \overline{(y + z)}$$

using (i) single 3-input AND gate and a NOT gate only ; (ii) minimum number of 2-input AND gates and a single NOT gate only ; (iii) 2-input NAND gates only.

4 + 4 + 2

- (b) Find the following :

3 + 3 + 4

(i) $(23.625)_{10} = (?)_8$

(ii) $(235.2)_{10} = (?)_4$

(iii) $(AFC4)_{16} \times (B9C)_{16} = (?)_{16}$

2. (a) Simplify and implement using minimum number of 2-input (i) OR and NAND gates, and (ii) NOR and OR gates.

$$\bar{F} = \bar{x}y + x\bar{y} + z$$

Use only 2-input gates such that total number of gates used is the smallest. 10

- (b) Design and implement a 2 bit by 2 bit binary multiplier using half adders. 10
3. (a) Using Tabular method, obtain prime implicate and minimal expression for

$$F = \pi M (2, 3, 8, 12, 13). d (10, 14). \quad 8$$

- (b) Implement using PLA: 6 + 6

$$F_1 (A, B, C) = \sum m (0, 1, 2, 4)$$

$$F_2 (A, B, C) = \sum m (0, 5, 6, 7)$$

4. (a) Consider two binary numbers represented as $A_1 A_0$ and $B_1 B_0$. Design a logic circuit whose output will be 1 when $A_1 A_0$ is equal to $B_1 B_0$. 10

- (b) Implement using 8×1 multiplier: 10

$$F = \sum m (1, 3, 4, 11, 12, 13, 14, 15)$$

Group B

5. Design and implement a pulse generator using a shift register to generate waveform representing

1 0 1 1 1 0 1 1 0 1 1 1 0 1

Use D flip-flop. 20

6. (a) Explain the limitations of finite state machines. Define, with examples, successor, terminal state, strongly connected machines. 8

- (b) Differentiate between Mealy and Moore models. 4

- (c) Reduce the machine to standard form for state table: 8

Ps	NS	
	X=0	X=1
A	E, 0	D, 1
B	F, 0	D, 0
C	E, 0	B, 1
D	F, 0	B, 0
E	C, 0	F, 1
F	B, 0	C, 0

7. (a) Design an asynchronous mod-10 counter using T flip-flops. 8

- (b) Design and implement a sequence detector which detects 1111. Overlapping sequences are allowed. Use D flip-flops. 12

8. (a) Explain the working of J-K master-slave flip-flop. Use only NAND gates. 10

- (b) Convert (i) D to J-K flip-flop, (ii) J-K to D flip-flop, and (iii) J-K to T flip-flop. 3 + 3 + 4

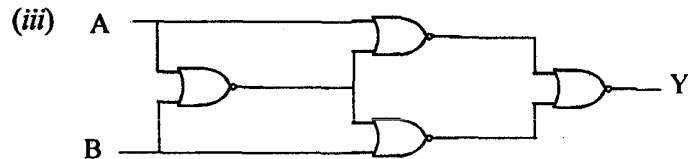
Group C

9. Choose the correct answer for the following: 10 x 2

- (i) The time required for a gate or inverter to change its state is called

- (a) rise time.

- (b) decay time.
 (c) propagation time.
 (d) charging time.
- (ii) The minimum number of two input NAND gates required to perform two input OR gate is
- (a) one.
 (b) two.
 (c) three.
 (d) four.



Output Y of the above logic function is

- (a) EX-OR
 (b) Ex-NOR
 (c) NAND
 (d) NOR
- (iv) Sum of full adders as output can also be obtained from ____.
- (a) three bit MUX.
 (b) three bit parity checker.
 (c) three bit comparator.
 (d) three bit counter.

- (v) To add 16 bit numbers, ____ half adders and ____ full adders are required, respectively.
- (a) 8, 8
 (b) 1, 15
 (c) 16, 0
 (d) 15, 1
- (vi) To construct a K-bit parallel adder, ____ number of full adders is required.
- (a) $K/2$
 (b) K
 (c) $K-1$
 (d) $K + 1$
- (vii) Minimum number of two input NAND gates required to implement $(\bar{A} + \bar{B})(C + D)$ is
- (a) 4
 (b) 2
 (c) 6
 (d) 5
- (viii) A two control input data selector can have ____ number of largest data inputs.
- (a) 2
 (b) 4
 (c) 6
 (d) 8
- (ix) In a ripple counter (JK triggered), the pulse input is applied to
- (a) clock of first flip-flop.
 (b) clock of last flip-flop.
 (c) J-K inputs of all flip-flops.
 (d) J-K input of first flip-flop.

- (x) If clock of period T is used with n stage shift register, then output of final stage will be delayed by
- (a) nT sec
 - (b) n/T sec
 - (c) $(2n + 1)T$ sec
 - (d) $(n-1)T$ sec

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