S.E. Sem # 4 (Rev.) Electronics - II 27/5/08.

632 : E-1stHI08. EXTC.

**Con. 3171-08.** **(REVISED COURSE)** **CO-9823**

(3 Hours) **[ Total Marks : 100**

**N.B.** (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions from **remaining**.
(3) Assume **suitable** additional data whenever **necessary**.

1. Design a two stage RC coupled BJT Amplifier to meet following specifications : **20**

   $A_v \geq 10000$ $S_{ICO} \leq 10$ $f_L = 25$ Hz $V_O = 2{\cdot}5$ V $V_{CC} = 12$ V

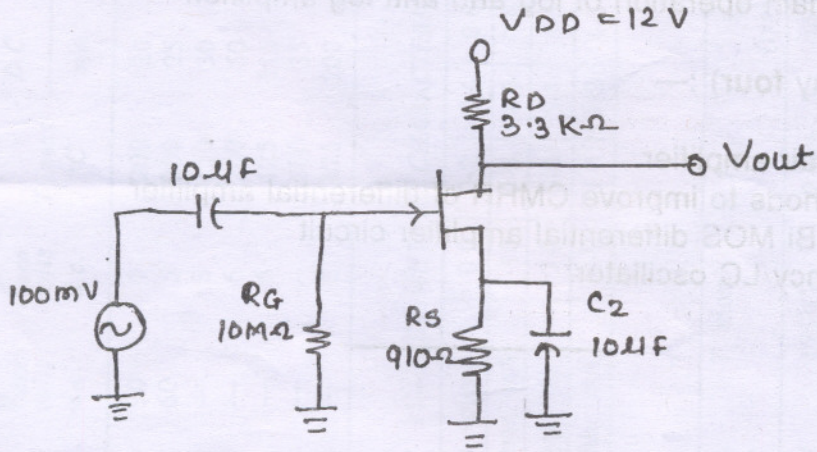
2. (a) Design a large signal class B power amplifier to provide 10 W output to the 4Ω load. **10**

   (b) Draw the circuit diagram using op-amps to realize $V_0 = 4\,V_1 - 3V_2 + 5\,V_3$. Explain the realization. **10**

3. (a) Draw the circuit diagram of temperature compensated log amplifier. Derive output expression. **10**

   (b) Explain with block diagram different topologies of negative feedback amplifier. What is improvement in $A_V$ and $A_I$ ? **10**

4. (a) (i) What is the total output voltage of the unloaded amplifier ? $I_{DSS} = 12$ mA, $I_D = 2$ mA, $V_{GS\,(OFF)} = -3$ V. **5**

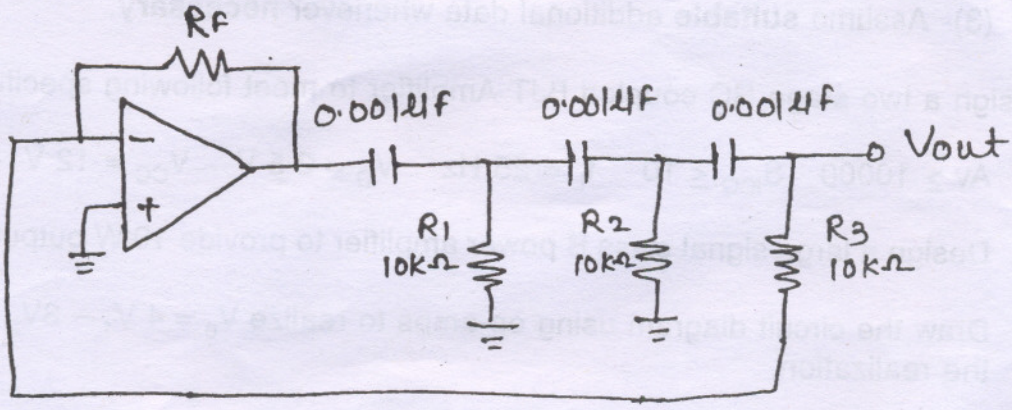



   (ii) Why the gate to source voltage of an N– channel JFET should always be either 0 or negatively biased ? **5**

   (b) Explain working and analysis of transformer coupled class A Power amplifier. **10**

**[ TURN OVER**

5. (a) (i) Determine value of $R_f$ necessary for the circuit to operate as an oscillator. **10**
   (ii) Determine frequency of oscillation.
   (iii) Why is the phase shift through the RC feedback circuit in a phase shift oscillator 180° ?




   (b) Draw the diagram of wien bridge oscillator and explain the operation. Derive expression for resonant frequency. **10**

6. (a) What are benefits of negative feedback in an op-amp circuit ? What are the effects of negative feedback on op-amp impedance ? **10**

   (b) Analyse and explain operation of log and anti log amplifier. **10**

7. Write short notes (any **four**) :— **20**
   (a) Heat sink
   (b) Darlington pair amplifier
   (c) Various methods to improve CMRR of differential amplifier
   (d) Bi FET and Bi MOS differential amplifier circuit
   (e) High frequency LC oscillator.

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# DBEC DATA SHEET

| Transistor type | Pdmax @ 25°C Watts | Icmax @ 25°C Amps | $V_{CE}^{(sat)}$ volts d.c. | $V_{CBO}$ volts d.c. | $V_{CEO}$ (Sus) volts d.c. | $V_{CER}$ (Sus) volts d.c. | $V_{CEX}$ volts d.c. | $V_{BEO}$ volts d.c. | $T_j$ max °C | D.C. current gain min | typ. | max. | Small Signal $h_{fe}$ min. | typ. | max. | $V_{BE}$ max. | $\theta_{jc}$ °C/W | Derate above 25°C W/°C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N 3055 | 115·5 | 15·0 | 1·1 | 100 | 60 | 70 | 90 | 7 | 200 | 20 | 50 | 70 | 15 | 50 | 120 | 1·8 | 1·5 | 0·7 |
| ECN 055 | 50·0 | 5·0 | 1·0 | 60 | 50 | 55 | 60 | 5 | 200 | 25 | 50 | 100 | 25 | 75 | 125 | 1·5 | 3·5 | 0·4 |
| ECN 149 | 30·0 | 4·0 | 1·0 | 50 | 40 | — | — | 8 | 150 | 30 | 50 | 110 | 33 | 60 | 115 | 1·2 | 4·0 | 0·3 |
| ECN 100 | 5·0 | 0·7 | 0·6 | 70 | 60 | 65 | — | 6 | 200 | 50 | 90 | 280 | 50 | 90 | 280 | 0·9 | 35 | 0·05 |
| BC147A | 0·25 | 0·1 | 0·25 | 50 | 45 | 50 | — | 6 | 125 | 115 | 180 | 220 | 125 | 220 | 260 | 0·9 | — | — |
| 2N 525(PNP ) | 0·225 | 0·5 | 0·25 | 85 | 30 | — | — | — | 100 | 35 | — | 65 | — | 45 | — | — | — | — |
| BC147B | 0·25 | 0·1 | 0·25 | 50 | 45 | 50 | — | 6 | 125 | 200 | 290 | 450 | 240 | 330 | 500 | 0·9 | — | — |

| Transistor type | hie | hoe | hre | θja |
|---|---|---|---|---|
| BC 147A | 2·7 K Ω | 18μ ℧ | 1·5 × $10^{-4}$ | 0·4°C/mw |
| 2N 525 (PNP) | 1·4 K Ω | 25μ ℧ | 3·2 × $10^{-4}$ | — |
| BC 147B | 4·5 K Ω | 30μ ℧ | 2 × $10^{-4}$ | 0·4°C/mw |
| ECN 100 | 500 Ω | — | —— | —— |
| ECN 149 | 250 Ω | — | —— | —— |
| ECN 055 | 100 Ω | — | —— | —— |
| 2N 3055 | 25 Ω | — | —— | —— |

*BFW 11—JFET MUTUAL CHARACTERISTICS*

| –VGS volts | 0·0 | 0·2 | 0·4 | 0·6 | 0·8 | 1·0 | 1·2 | 1·6 | 2·0 | 2·4 | 2·5 | 3·0 | 3·5 | 4·0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IDS max. mA | 10 | 9·0 | 8·3 | 7·6 | 6·8 | 6·1 | 5·4 | 4·2 | 3·1 | 2·2 | 2·0 | 1·1 | 0·5 | 0·0 |
| IDS typ. mA | 7·0 | 6·0 | 5·4 | 4·6 | 4·0 | 3·3 | 2·7 | 1·7 | 0·8 | 0·2 | 0·0 | 0·0 | 0·0 | 0·0 |
| IDS min. mA | 4·0 | 3·0 | 2·2 | 1·6 | 1·0 | 0·5 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 |

N-Channel *JFET*

| Type | $V_{DS}$ max. Volts | $V_{DG}$ max. Volts | $V_{GS}$ max. Volts | $P_d$ max. @25°C | $T_j$ max. | $I_{DSS}$ | $g_{mo}$ (typical) | $-V_P$ Volts | $r_d$ | Derate above 25°C | $\theta_{ja}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N3822 | 50 | 50 | 50 | 300 mW | 175°C | 2 mA | 3000 μ ℧ | 6 | 50 KΩ | 2 mW/°C | 0·59°C/mW |
| BFW 11 (typical) | 30 | 30 | 30 | 300 mW | 200°C | 7 mA | 5600 μ ℧ | 2·5 | 50 KΩ | —— | 0·59° C/mW |