GUJARAT TECHNOLOGICAL UNIVERSITY
B.E. Sem-III Examination December 2009
Subject code: 130704
Subject Name: Computer Organization and Architecture
Date: 29 / 12 /2009   **Time: 11.00 am – 1.30 pm**
Total Marks: 70

Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following questions.   **07**
      1. What is register transfer language? Clear it with example.
      2. Explain the operation of three state bus buffers and show its use in design of common bus.

      (b) Explain the direct and indirect address with example and compare them. **07**

Q.2 **(a)** Draw the circuit for control unit of basic computer and explain its working. **07**

      (b) What do you mean by completeness of instruction set? Give the reasons to choose the instructions in each category. **07**

OR
      (b) Write a program loop using a pointer and a counter to clear the contents of hex locations 500 to 5FF with 0. **07**

Q.3 **(a)** Compare the following.   **07**
      1. Microprogrammed and hardwired control organization.
      2. Register reference and memory reference instructions.

      (b) Describe the first pass of assembler with the help of flowchart and show how symbol table is generated using an example. **07**

OR
Q.3 **(a)** What is program interrupt? What happens when it comes? What are the tasks to be performed by service routine? **07**

      (b) Describe the following terms with proper example in each case: micro operation, microinstruction, microprogram, microcode. **07**

Q.4 **(a)** What is stack? Give the organization of register stack with all necessary elements and explain the working of push and pop operations. **07**

      (b) List the important characteristics of RISC architecture and explain the use of overlapped register windows. **07**

OR
Q.4 **(a)** What are the flag bits? Give the meaning of each and use of them in programming. **07**

      (b) Explain the following. **07**
      1.Data transfer instructions. 2.Flynn's classification of computers.

Q.5 **(a)** What are the pipeline conflicts? Explain the hardware techniques to handle the branch instructions. **07**

      (b) Multiply the (-8) with (12) using Booth's algorithm. Give each step. **07**

OR
Q.5 **(a)** Considering three segment instruction pipeline, illustrate the concepts of delayed load and delayed branch with example. **07**

      (b) Explain the Booth's algorithm with the help of flowchart. **07**

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