Code: CS12 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

MARCH 2011

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 **(7×4)**

a. Explain the organisation of Ist generation computer.

b. How is performance of a computer related to execution time? Explain performance equation.

c. Explain important registers and their use in a CPU.

d. Realise the following functions using PLA

$X = \overline{A}\,\overline{B}\,C + A\overline{B}\,\overline{C} + \overline{B}\,C$

$Y = \overline{A}\,\overline{B}\,C + A\overline{B}\,\overline{C}$

$Z = \overline{B}\,C$

e. Draw the logic diagram and truth table for a 4 to 2 bit priority encoder.

f. Explain Instruction cycle.

g. What do you mean by I/O mapped I/O and memory mapped I/O.

Q.2 a. Multiply 5 with -4 using Booth's algorithm. **(9)**

b. Write the code to execute $X = (A \times B) + (C \times C)$ using 3 address, 2 address, 1 address and 0 address instruction format. **(9)**

Q.3 a. Design a hardware control unit to add two 32 bit numbers using a 4 bit binary adder. Assume each register is of 4 bit only. Sequence counter is to be used to control the process. **(9)**

b. Using non restoring division algorithm for the unsigned numbers, show the data flow at each stage for dividing $(1010)_2$ with $(0011)_2$. **(9)**

Q.4 a. What is microprogramming? Explain vertical and horizontal micro programmed controller. **(9)**

b. Explain the operation of instruction pipelines and the pipeline structure in RISC. **(9)**

Q.5 a. Draw the organisational structure of a 2D 4MB memory constructed using $256\,K \times 1$ chip. **(9)**

b. A computer has 16 MB main memory and 64 KB cache. The block size is 16 bytes.
(i) How many cache lines does the computer have
(ii) How many blocks does the main memory have
(iii) Give the starting address of memory blocks which are directly mapped to cache lines
(iv) Explain how a given address is retrieved from the memory system. **(9)**

Q.6 a. Explain with diagrams the concept of programmed I/O. **(9)**

b. Explain software polling, daisy chaining and vectored interrupt method of data transfer. **(9)**

Q.7 a. Discuss the optimization criteria's in designing a computer system. **(9)**

b. Write short notes on any **THREE**:- **(3 × 3)**

(i) RISC Vs CISC
(ii) Virtual memory
(iii) DMA data transfer
(iv) Speed up features of modern computers.