MARCH 2010

ALCCS

Code: CS12 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 Choose the correct or best alternatives: (7 × 4)

a. Given a 32 × 8 ROM chip with an enable input, show the external connection necessary to construct a 128 × 8 ROM with four chips and a decoder.

b. Draw a 4 bit adder subtractor using 4 full adders. An input signal when 0, makes it an adder and when signal is 1, makes it a subtractor.

c. Briefly explain a 2 pass assembler.

d. Write in reverse Polish notation
(A+B) * [C * (D+E)+F]

e. The cache memory of 2 K words uses direct mapping with a block size of 8 words. How many blocks can the cache accommodate?

f. What is the difference between a micro-instruction and a micro-code

g. Write a note on virtual memory.

Q.2 a. Design a four bit priority encoder consisting of four lines P, Q, R & S. R has highest priority followed by P, S and Q. State an application of the priority encoder.

b. With neat block diagram explain the operation of a 4 bit combinational array multiplier. Illustrate the data flow in that array multiplier while multiplying $x = (1010)_2$ and $y = (0011)_2$. **(8+10)**

Q.3 a. What is a macro? How it is used as a tool for simplifying program design? How it is different from subroutine?

b. Discuss the characteristic features of RISC and CISC Processor. State the situations in which RISC and CISC processors are preferable. **(8+10)**

Q.4 a. With neat block diagram explain the operation of a microprogram sequencer.

b. Discuss the design methodology used for designing hardware control unit. State the advantages of hardware control unit over microprogrammed control unit. **(8+10)**

Q.5 a. Explain the following terms:-

(i) Effective address. (ii) Logical address.
(iii) Virtual address. (iv) Physical address.

b. Explain the various page replacement policies with reference to the memory management.

c. Analyse the effect of block size on Hit ratio. **(8+5+5)**

Q.6 a. Use the Booth multiplication Algorithm to multiply 8 with – 4.

b. Describe briefly the organization of the memory mapping table in a paged system in the context of virtual memory.

c. Discuss the Methodology / techniques used for serial and parallel data transfer between two computer systems. **(5+8+5)**

Q.7 Write short notes on:-

(i) Set- associative mapping
(ii) Polling
(iii) Handling interrupt priorities. **(6 × 3)**