Code: AE13 **Subject: COMPUTER ENGINEERING**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2007

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. If the memory addressing capability of the CPU is equal to 4K, the number of address lines of the CPU is

(A) 8 **(B)** 14
(C) 12 **(D)** 4

b. The value of the hexadecimal number E9H in binary is

(A) 1001 1110 **(B)** 0101 1100
(C) 1100 1101 **(D)** 1110 1001

c. The two's complement signed binary number is given by 10110101. Its decimal equivalent is

(A) +45 **(B)** +75
(C) –75 **(D)** +65

d. The crystal frequency required for an 8085 microprocessor based system to operate at 1.1 MHZ is

(A) 8.8 MHz **(B)** 3.3 MHz
(C) 1.1 MHz **(D)** 2.2 MHz

e. Assume the accumulator holds the data byte FFH. After executing the instruction ADI 01H, the sign flag, zero flag and carry flag in 8085 would be

(A) 0, 1, 1 **(B)** 1, 0, 0
(C) 0, 1, 0 **(D)** 1, 1, 0

f. The storage cell of a DRAM is actually a

(A) Inductor **(B)** Diode
(C) Capacitor **(D)** None of the above

g. In 8251 (USART) the mode word CAH indicates the character length to be transmitted is

(A) 5-bit character **(B)** 6-bit character
(C) 4-bit character **(D)** 7-bit character

h. If the full 4GB of the 486's memory space is cached with a 128 KB of SRAM, the TAG SRAM needs to be how many bits wide

(A) Eleven **(B)** Six
(C) Fifteen **(D)** None

i. The PCI bus connects to the processor via the following

(A) RS-232C **(B)** Adapter
(C) PCI bridge **(D)** ISA bus

j. The mode that allows the transmission in only one direction is

(A) Simplex **(B)** Full duplex
(C) Parallel **(D)** Half duplex

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Discuss the working principle of a pipelined computer, give examples of some pipelined computers. **(8)**

b. Discuss Flynn's classification of computers with examples. **(8)**

Q.3 a. Compare the Decimal and Binary number systems with suitable example. **(8)**

b. Convert the number 483 to binary using the repeated-subtraction method. **(4)**

c. Assume the following bytes have been received over a serial data line: E1H, 20H, 72H. If these bytes were encoded using even parity, which if any, are in error? **(4)**

Q.4 a. Give the 8086 microprocessor programming model and explain the 8086 flag word? **(8)**

b. Write an 8085 microprocessor program to count from 0 to 9 (modulo ten) with a one-second delay between each count. Assume the clock frequency of the microprocessor is 1 MHz. **(8)**

Q.5 a. Explain the different types of optical disks in detail with the help of relevant figures. **(8)**

b. Illustrate a diode ROM with n-input address decoder, 2^n x m memory array and m output buffers and explain. **(8)**

Q.6 a. Draw the 8279 logic block diagram and explain. **(8)**

b. Explain the control word of 8255A and write an 8085 Assembly language program to read the DIP switches and display the reading from port B at port A and from port C_L at port C_U. (Assume your own address decoding logic)? **(8)**

Q.7 a. With a neat block diagram of 8259A explain the sequence of events that occur when one or more interrupt request lines go high after the 8259A has been initialized. **(8)**

b. Write a program including the initialization of the USART(8251) to transmit a message (stored as ASCII characters without parity in memory locations starting at XX70H) from an 8085 single board microcomputer to a CRT terminal. The program should check the status before it transmit a character. **(8)**

Q.8 a. Draw the 80386 microprocessor model and explain its BIU, CPU and MMU? **(8)**

b. Explain the following in a Pentium microprocessor
(i) The u and v pipes
(ii) Floating-point unit
(iii) Cache unit **(3+3+2)**

Q.9 a. Describe the architecture of the 8-bit PC and XT computers. **(8)**

b. Show how the 8255A PPI chip can be interfaced to the I/O bus of the PC/XT so that the chip is mapped to ports 3FC–3FFH. What are the commands to program the chip for mode 0 operation with ports A and B operating as input ports and port C as an output port? **(8)**