Code: A-13 **Subject: COMPUTER ENGINEERING**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x8)

a. The process of conversion of a whole decimal number to any other base is accomplished by

(A) dividing by the radix. **(B)** multiplying by the radix.
(C) adding to the radix. **(D)** subtracting to the radix.

b. The write cycle time of a memory is 200 ns. The maximum rate at which data can be stored in this memory is

(A) 200 words/sec **(B)** 5000 words/sec
(C) 5×10^{6} words/sec **(D)** 5×10^{8} words/sec

c. When 8086 μp is reset the address bus contains

(A) 0000H **(B)** $\overline{\text{F000H}}$
(C) 0034H **(D)** 003CH

d. The driver IC used to convert RS 232-C signal levels to TTL levels is

(B) MC 1489. **(B)** MC 1488.
(C) MC 3487. **(D)** MC 3486.

e. ISA bus has

(A) 24 address lines and 16 data lines.
(B) 24 address lines and 24 data lines.
(C) 16 address lines and 16 data lines.
(D) 16 address lines and 8 data lines.

f. The addressing mode of the instruction `LXI H, 2080` is

(A) Register addressing mode.
(B) Immediate addressing mode.

(C) Register indirect addressing mode.
(D) Relative address addressing mode.

g. The Content Addressable Memories (CAM) are also called

(A) Associative memories. **(B)** Cache memories.
(C) Virtual memory. **(D)** Segmented memory.

h. SIMMs (Single In-line Memory Modules) are available in

(A) 64 pins. **(B)** 72 pins.
(C) 128 pins. **(D)** 168 pins.

PART I
Answer any THREE Questions. Each question carries 14 marks.

Q.2 a. Write the number 2_{10} in binary form and then subtract 7_{10} from it using 2's complement technique. **(3)**

b. Find the decimal equivalent of hexadecimal number 2BA5. **(2)**

c. What are self-complementing codes? **(2)**

d. Why is BCD code called a weighted 8421 code? **(2)**

e. Write down the method (steps) to convert a binary number to a Gray code. **(3)**

f. Write down the difference between intelligent and dumb terminals. **(2)**

Q.3 a. Describe the structure of a DRAM cell. Explain how refreshing is performed in DRAM. **(4)**

b. A processor has 16-bits of address and 8-bit data lines. Memory chips are available each of $16K \times 8$ bits. How many chips are needed and how to connect them in the system to avail full memory capacity? **(4)**

c. Explain the following with respect to cache memory:
(i) Locality of reference.
(ii) Hit ratio.
(iii) Write through. **(6)**

Q.4 a. Draw and explain the timing diagram of the 8085 instruction IN 05H. **(8)**

b. For the program given below:

Instruction	No. of T-states
XRA A	4
LXI B 4612	10

```
        LXI H 0020      10
L1:     DCX H           6
        JNZ L1          10
        INR B           4
```

(i) Calculate the time to execute the above program if clock frequency is 1 MHz.
(ii) What will be the contents of HL pair and BC pair after the execution of above program. **(6)**

Q.5 a. Draw the block diagram of 80386 CPU. Explain briefly the operation of each unit. **(8)**

b. List down atleast four features of Pentium series of processors. **(6)**

Q.6 Justify the following statements:

(i) RS 232 is a 25 pin serial I/O voltage standard compatible with TTL logic. **(3)**

(ii) The execution of the following instructions will enable all the three interrupts (RST 7.5, RST 6.5 and RST 5.5).

```
EI
MVI A 10H
SIM
```

(3)

(iii) 8255 can be used in mode 2 to transfer the data between two computers. **(3)**

(iv) The hardware approach to interface a matrix keyboard and multiplexed seven segment display using 8279 is advantageous to the software approach. **(3)**

(v) DMA controller 8237 works only in Master mode. **(2)**

PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. What is an addressing mode? Explain various addressing modes of 8086 with examples. **(6)**

b. Explain the following instructions with reference to 8085.

(i) CMP M. (ii) PCHL.
(iii) LHLD 8020H. (iv) LDAX B 4060H. **(8)**

Q.8 a. What do you mean by pipelined architecture? How is it implemented in 8086? **(6)**

b. Explain the role of following signals of 8086 in minimum mode and in maximum mode.

(i) S_0, S_1 and S_2. (ii) $\overline{RQ_0}/GT_0$ and $\overline{RQ_1}/GT_1$. **(4)**

c. Explain the interrupt structure of 8086. **(4)**

Q.9 a. Answer the following with respect to UNIX:

(i) What are the functions of Kernel?
(ii) What is a shell?

(iii) What facilities are provided by outer most layer of UNIX OS?
(iv) What are UNIX pipes?
(v) What are UNIX filters? **(10)**

b. What are the functions of a BIOS in PC's? **(4)**

Q.10 a. Write a program in 8085 assembly language to sort ten numbers in ascending order. **(4)**

b. Write the control word and assembly language program to generate a 1 KHz square wave from counter 2 of 8253 / 8254. Assume that gate input of counter 2 is tied to +5V through 10 K resistor and the clock input of counter 2 is connected to 2 MHz. **(5)**

c. What is the difference between synchronous and asynchronous serial communication. Explain the following terms w.r.t. serial communication
(i) framing error. (ii) full duplex.
(iii) baud rate. **(5)**

Q.11 a. Write down the salient features of EISA bus. **(5)**

b. Explain the following in brief (any **THREE**):

(i) RAID.
(ii) Dot Matrix Printer.
(iii) Power PC.
(iv) Optical Scanners.
(9)