

# SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E - EEE

Title of the paper: Computer Aided Design

Semester: V

Sub.Code: 414507

Date: 13-11-2008

Max. Marks: 80

Time: 3 Hours

Session: FN

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## PART – A

(10 x 2 = 20)

Answer All the Questions

1. What are the various control flow structures?
2. Define Simulink applicable to Mat Lab.
3. Define Nodal analysis with example.
4. What do you mean by DFT and FFT sequence?
5. What are the characteristics of full wave rectifier?
6. What is the importance of Transfer function?
7. Differentiate the basic identifier and extended identifier.
8. Differentiate the concurrent and sequential signal assignment statements.
9. Why are configurations needed?
10. Define the term attribute with an example.

## PART – B

(5 x 12 = 60)

Answer All the Questions

11. Explain with suitable example the basic data analysis.  
(or)
12. Explain in detail the M-file function construction rules.

13. For the electrical system shown in figure-1. Assume that  $R_1 = 1.5\Omega$ ,  $R_2 = 1\text{ M}\Omega$ ,  $C_1 = 0.75\ \mu\text{F}$  and  $C_2 = 0.2\ \mu\text{F}$  and the capacitors are not charged initially and  $e_0(0) = 0$  and  $e_0 = 0$ .
- Find the response  $e_0(t) = 6\text{V}$  (step input) is applied to the system.
  - Plot the response curve  $e_0(t)$  versus  $t$  using Mat lab (write programme)

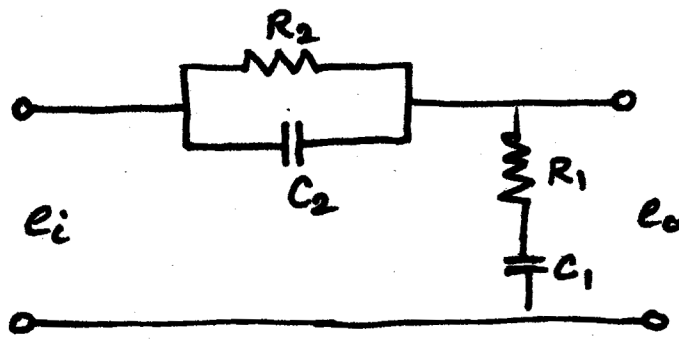


Figure - 1

(or)

- With suitable example explain the Z, Y, H Two port networking parameter analysis.
  - Distinguish the open loop and close loop transfer function with suitable example.
- (or)
- Explain the following
    - BJT
    - MOSFET
    - Zener Diode.
  - Explain in detail the multiple drivers with an example.
- (or)
- Explain the structural model of a decade counter using j.k flip-flops
  - Explain with example the various types of Subprograms.
- (or)
- What is generate statement? Explain the 4 bit full adder using generate statement.