AMIETE – ET (OLD SCHEME)

Code: AE27 **JUNE 2009** **Subject: DIGITAL HARDWARE DESIGN**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. An electronic circuit in which a state switches between two distinct states when there is a change in the input states or conditions is called
(A) Digital circuit. **(B)** Analog circuit.
(C) Mixed circuit. **(D)** None of the above.

b. If an entity is a gate level model with a rise and fall delay, values for the rise and fall delays could be passed into the entity using
(A) Driver. **(B)** Bus.
(C) Generics. **(D)** Process.

c. VHDL stands for
(A) Verilog Hardware Description Language.
(B) Very High Speed Digital Language.
(C) Versatile Hardware Description Language.
(D) Very High Speed Integrated Circuit Hardware Description Language.

d. The ASSERT statement in VHDL checks the value of a
(A) Boolean Expressions. **(B)** Complex Expressions.
(C) Textual String. **(D)** Both **(A)** and **(B).**

e. In an VHDL, signal represents the
(A) Interconnection wires. **(B)** Components.
(C) Ports. **(D)** Temporary data.

f. $(XY)_5=(YX)_4$, then
(A) X=4, Y=3. **(B)** X=4, Y=3.
(C) X=6, Y=3. **(D)** X=3, Y=4.

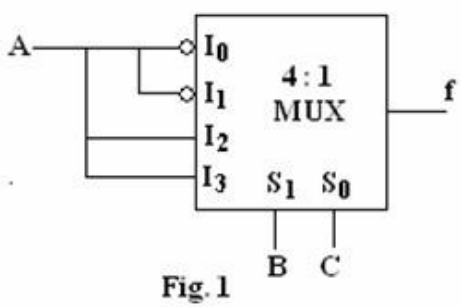


Fig. 1

g. Implementation of a switching function through a 4:1 MUX is shown in Fig.1. Identify the switching function

(A) $\Sigma(0,1,6,7)$
(B) $\Sigma(2,4,6,7)$
(C) $\Sigma(1,3,5,6)$
(D) $\Sigma(4,5,6,7)$

h. If $M(H)$ and $M(\overline{H})$ denote the convex hulls of the sets of True and False vertices of a function H respectively, then if $M(H) \cap M(\overline{H}) = \phi$, where ϕ denotes the empty set, then the said function is
(A) Threshold function. **(B)** Symmetric function.
(C) Unate function. **(D)** Walsh function.

i. An N-bit Jhonson counter generates a counting sequence of length.
(A) N/2 **(B)** 1
(C) N **(D)** 2N

j. In FPLA
(A) Only AND arrays are programmable.
(B) Only OR arrays are programmable.
(C) Both the AND array and the OR array are programmable.
(D) None of these are programmable.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. List the advantages and disadvantages of a digital circuit over an analog circuit. **(4)**

b. Prove X + (Y Z) = (X + Y) (X + Z) = (X + Y) (X + Y + Z). **(4)**

c. Simplify A . C + A . (C + B) + C . (C + B) using Boolean algebra and Realize the simplest possible circuit. **(4)**

d. Convert (A+B+C).(A+D) expression into standard Product Of Sum form. **(4)**

Q.3 a. Explain the method to determine the given function is symmetric. **(4)**

b. Determine which of the following functions is symmetric and identify its numbers and variables of symmetry. **(4)**

$f(X,Y,Z) = \Sigma(1,2,4,7)$

c. Write a short note on Symmetric Networks. **(4)**

d. Determine whether the function f (x1, x2, x3, x4) = Σ (0, 1, 3, 4, 5, 6, 7, 12, 13) is a threshold function, and if it is, find a weight-threshold vector. **(4)**

Q.4 a. Convert the following Mealy machine to an equivalent Moore machine. **(8)**

Present State	Next State, Output	
	X=0	X=1
A	C, 0	B, 0
B	A, 1	D, 0
C	B, 1	A, 1
D	D, 1	C, 0

b. Write a VHDL code for simple MUX by using structural and data-flow styles. **(4)**

c. Write a short notes on:

(i) Guarded Blocks.
(ii) Block Statements. **(4)**

Q.5 a. Given a logic design and implementation using the multiplexers for F1= Σ (3, 7) using a 4:1 multiplexer. **(4)**

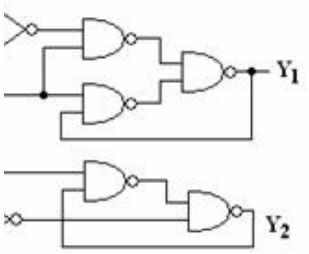
b. Explain a 4-bit adder cum subtraction circuit, which uses the XORs as a controlled inverter. **(4)**

c. Explain the difference between a decoder and a digital multiplexer? Describe four applications of a decoder. **(4)**

d. Explain a parallel in serial out (PISO) left shift register using a state table. **(4)**

Q.6 a. Define a fundamental mode and pulse mode of operations for a sequential machine **(4)**

b. Compare Moore model and Mealy model with example. **(4)**



c. For the Logic Circuit, construct transition. Table and determine all critical races and non-critical races. Explore the possibility of cycles. **(8)**

Q.7 a. Discuss the FPGA based design flow and specify the different tools available in the market for each abstraction level. **(4)**

b. Write the VHDL Code for D flip-flop with asynchronous clear and preset using behavioural approach. **(4)**

c. Write a VHDL code for one bit full adder using data flow architecture. Extend it to 4-bit adder using structural approach. **(4)**

d. List the differences between variable and signals. Explain with one example. **(4)**

Q.8 Write short notes on the following: **(16)**
(i) Hazards and Races
(ii) GAL devices
(iii) CAD tools in digital system design
(iv) Mixed style of Modelling in VHDL

Q.9 a. Draw ASM chart of a serial adder and synthesize the Logic circuit. **(8)**

b. Explain the concept of microprogramming. Describe the "Horizontal microprogramming" and "vertical microprogramming. **(8)**